Power Module Condition Monitoring for Offshore Wind Applications with Focus on the Die Attach Degradation

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Abbreviations and Symbols

1D	One-dimensional	A	Area; if used as unit it refers to Amp
2D	Two-dimensional	C	Capacitance or capacitor in a circuit
3D	Three-dimensional	C_{th}	Thermal capacitance
ANN	Artificial Neural Network	cos φ	Cosine of the phase angle between voltage and current (in the IGBT)
C	Collector terminal (positive) of IGBT	d	Thickness (of chip)
CAPEX	Capital expenditure	ΔTj	Change of the junction temperature
CTE	Coefficient of thermal expansion	ΔTc-a	Change of the case-to-ambient temperature difference
DAQ	Data Acquisition	ΔTj-c	Change of the junction-to-case temperature difference
DBC	Direct Bonded Copper (substrate of IGBT modules)	dT	Temperature spatial gradient
DFIG	Doubly-fed induction generator	dx	Distance in the direction x (of heat flow)
DUT	Device under test	E_{OFF}	Energy (loss) at turn-OFF
E	Emitter terminal (negative) of IGBT	E_{ON}	Energy (loss) at turn-ON
EOS	Electrical overstress	f_{sw}	Switching frequency
ESD	Electrostatic discharge	I	Current
FEA	Finite element analysis	i_L	Current (sinusoidal) through inductor or load
FEM	Finite element method	I_{ph}	Phase current

G	Gate terminal (of IGBT)	k	Thermal conductivity of a material [W/mK]
GTO	Gate turn-off thyristor	P_d	Power dissipation (loss)
HPL	Healthy (ideal) power losses	P_{loss}	Power loss
IGBT	Operational power losses	P_{tot}	Total power loss
IGCT	Integrated gate-commutated thyristor	q	Local heat flux density [W/m^2]
KTP	Knowledge transfer partnership	R	Resistance or resistor in a circuit
LCOE	Levelised cost of energy	RC	Resistor –capacitor (network or filter)
LUT	Look-up table	R_{CE}	Electrical resistance between collector and emitter
M1-B	Module 1 bottom IGBT chip	R_{th}	Thermal resistance
M1-T	Module 1 top IGBT chip	s	Symbol denoting volumetric heat capacity of a material
M2-B	Module 2 bottom IGBT chip	T	Temperature
M2-T	Module 2 top IGBT chip	T_a	Ambient temperature
M3-B	Module 3 bottom IGBT chip	τ (tau)	Time constant associated with RC networks
M3-T	Module 3 top IGBT chip	T_c	Temperature of the power module case (baseplate or DBC)
MOS	Metal-oxide-semiconductor	T_{c-a}	Difference between the case and the ambient temperature
MOSFET	Metal-oxide-semiconductor field-effect transistor	T_j	Junction temperature
O&M	Operation and maintenance	$T_{j\ ave}$	Average junction temperature

OPEX	Operational expenditure	V	Volatge (or the unit volt)
OPL	Operational (actual) power losses	V_{CE}	Collector emitter voltage (of IGBT)
PF	Power factor	V_{CE}/dt	The rate of change of V_{CE} with time
PiN	Describing diode with an intrinsic middle layer	V_{CEsat}	Collector-emitter saturation voltage
RBSOA	Reverse bias safe operating area	V_f	Forward voltage (of a diode)
ROC	Renewable Obligation Certificate(s)	V_{out}	Voltage out
SCADA	Supervisory control and data acquisition (system)	Z_{th}	Thermal impedance
SOA	Safe operating area	E_{rr}	Reverse recovery energy (loss) of a diode
TDDB	Time-dependent dielectric breakdown	P_{cond}	Conduction power loss
TSEP	Temperature sensitive electrical parameters	P_{ON}	Power loss at turn-ON
VSC	Voltage source converter	P_{OFF}	Power loss at turn-OFF
WMG	Warwick Manufacturing Group	V_{DC}	Converter DC link voltage
ZTC	Zero temperature coefficient		

Declaration

This thesis is submitted to the University of Warwick in support of the application for the degree of Doctor of Philosophy. It has not been submitted in part, or in whole, for a degree or other qualification at any other University. Parts of this thesis are published by the author in peer-reviewed research papers listed. Apart from commonly understood and accepted ideas, or where reference is made to the work of others, the work described in this thesis is carried out by the author in School of Engineering of the University of Warwick.

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Abstract

This thesis documents the research for a field-deployable on-line condition monitoring method which can be applied to the IGBT modules inside power electronic converters in offshore wind turbines. The main focus is on determining the health condition of the module packaging and on finding a viable means for tracking its gradual in-service degradation. Of the two main packaging degradation mechanisms – solder fatigue and bond-wire lift off – greater attention is paid to the former, although the researched condition monitoring method may also allow the detection of the latter. The signature considered here as most indicative of module degradation is the increase of its internal power loss for the same electrical operating point (defined by current level, power factor, switching frequency, etc.). Power loss and junction temperature affect each other in a circular fashion, progressively increasing, especially when the heat flow path to the outside cooling system is compromised by increasing levels of solder fatigue. The method explored here for assessing the device power losses in operation relies on external case and heat sink temperature signals and the novel use of ANNs in place of a thermal model. Although the explored concept is not yet ready for industrial use, it shows potential for further development. Power loss modelling with thermal feed-back is undertaken to develop a better understanding of the devices' operation. Special focus is paid to the current sharing and temperature profiles of paralleled chips inside the same packaging experiencing different degradation levels. High resolution scans of the die-attach solder layer of power cycled modules are also performed to gain understanding of their degradation.

Chapter

1 Introduction

1.1 UK's Cost Goals for Offshore Wind

With the issue of climate change becoming a worldwide concern, governments are pursuing policies aiming to increase the share of renewables in their total energy mix. UK's target for year 2020 is 15% of its total energy to be supplied from renewable energy sources and offshore wind alone is expected to deliver between 14 and 25% of that [1]. In the European context, UK is at the forefront of the offshore wind sector with about 50% of the entire European installed capacity. According to a report by the UK Government's Department for Business, Energy & Industrial Strategy in the first quarter of 2016, UK's offshore wind installed capacity is about 5.6 GW and its contribution to the total amount of electricity generated from renewable energy sources is around 20% [2].

This puts offshore wind in a top position amongst a group of 8 renewable energy technologies on which the UK government has selected to focus its support due to their cost effectiveness, potential for deployment and therefore high importance for meeting UK's 2020 and 2050 energy strategy targets [1]. Offshore wind can potentially deliver higher energy yields than most of the other technologies in this group. Its planning restrictions are not as onerous as the ones for onshore wind for which the good sites for development are almost exhausted. However, in terms of economic viability, offshore wind still cannot compete with other low carbon technologies such as nuclear power. Therefore, it also faces the challenge to bring down its Levelised Cost of Energy (LCOE) by 30% or to around £100 per MWh by 2020 [1].

The LCOE of offshore wind as given in [3] is around £140 per MWh. The average price which the offshore wind farm operators are getting per MWh, including the ROC incentive value, is also around £140 per MWh (information collected from e-mails and communications with offshore wind energy consultants at ORE Catapult (Blyth), formerly known as Narec, 2013-2014). This indicates that currently most offshore wind farm operators are likely to be running on very slim profit/loss margins. In such a situation any uncertainties (such as expected downtime and need for maintenance) in the running costs of offshore wind farms can render the entire offshore wind projects financially unsuccessful, thus making this relatively new industry seem risky and less inviting for potential investors.

To achieve the offshore wind LCOE reduction target, any opportunity for lowering the costs of generating offshore wind power should be explored and utilised. The capital expenditure (CAPEX) of offshore wind farms accounts for the greater portion of the LCOE [3]– about 60% (including cost of foundations, substations, subsea cables, etc.) Those costs can be reduced to a certain extent due to economies of scale, but ultimately there is a limit imposed by the cost of the raw materials.

The operating expenditure (OPEX) accounts for about 35-37% of the total LCOE of offshore wind [3]. A small part of this are set rates (seabed lease, transmission power cables, etc.) that do not hold much potential for cost reduction. But the larger part of the OPEX is associated with the operation and maintenance (O&M) costs which account for 18–23% of the total cost of offshore wind energy. Estimates by GL Garrad Hassan for the growth of the offshore wind O&M industry indicate that by 2025 in the UK alone it would reach over £2bn per annum [4], meaning that the O&M is likely to be an undesirably large running cost for the offshore wind farm operators. The O&M cost is that unlike the one-off CAPEX, runs throughout the whole lifetime and it is a variable cost dependent on uncertainties that may be impossible to accurately plan for in advance. Yet, its very variability means that it holds higher potential for optimisation than other costs which are set. Thus, reducing the O&M costs is likely to play a significant role in reducing the overall LCOE of offshore wind.

To reduce O&M costs in general we need to look into reducing the need for maintenance on the one hand (i.e. improving the system's reliability) and optimising maintenance strategies on the other hand (i.e. reducing the number of trips for the same the amount of servicing work, etc.) Both of these directions of work can benefit from the use of condition monitoring. It can provide visibility over a system's or a component's health condition during operation and thus advise on whether or not it operates reliably and whether or not it needs maintenance. In fact, condition monitoring of some wind turbine subassemblies such as the gearbox and the rotor blades has already proved successful in reducing maintenance cost and preventing catastrophic failure and is now included as a standard feature in modern wind turbine controllers. However, condition monitoring for the wind turbine's power electronic converter is still an underdeveloped field. This is why, in the wider context of looking for means to reduce the LCOE and contribute to the growth of offshore wind, the current research project has opted to focus on this topic.

1.2 Difference between Onshore and Offshore O&M

One may ask why condition monitoring for all wind turbine subassemblies has not been developed yet. The answer to this is that the cost of not having it has not been high enough so far. Indeed, the subassemblies for which there already exists condition monitoring in onshore wind turbines are only the ones that are

most expensive to replace or repair (e.g. gear box, rotor, bearings.) With the move of the wind industry offshore, however, all maintenance becomes not only much more expensive, but also much more difficult. As a Supergen Wind technology survey [5] sums it up, condition monitoring can be beneficial onshore, especially for larger wind turbines, but it is nothing less than essential for offshore wind development. This is because the traditional O&M strategies used onshore are no longer cost effective offshore and to be competitive offshore wind must develop new approach towards O&M.

Onshore for less cost-critical subassemblies (such as the power electronic converter) the maintenance is predominantly reactive – i.e. in answer to failure that has occurred. Still, because they are relatively cheap and easy to repair/replace the downtime associated with individual failures can be kept fairly short (often in the order of hours). The average availability of onshore turbines remains relatively high – around 95% [6]. Thus, there is no strong industry driven incentive to improve tried and tested designs and maintenance routines, as any change could result in extra cost (at least initially). With the move offshore, however, the extra cost to improve the reliability of the technology and the scheduling of maintenance can now be justified.

Access to offshore wind turbines is often problematic due to adverse weather conditions. Thus, any unpredictable breakdowns they experience can lead to prolonged downtimes, meaning substantial losses of expected revenue for the operator. Although there is yet little statistical data about the reliability and

downtime of offshore wind turbines, some publications looking at the early-years operation reports of several near-shore windfarms [7], [8] indicate that their availability has been worse than expected, highly dependent on the weather conditions and in general much lower than the average availability of onshore wind farms. The nearshore wind farm locations (UK Round 1 sites) are only up to 10 km away from shore with water depth up to 20 m. As those sites are now being exhausted and offshore wind move further and further away from shore (UK Round 2 and Round 3 sites) the problems arising from poor accessibility are only expected to escalate. For example, Dogger Bank Teeside A – a Round 3 site with authorised consent for wind farm development – is at a distance of 196 km or 214 km (as computed from the centre of the site) away from the nearest North Yorkshire shore [9], [10]. Naturally, the transportation costs to and from such a site will be already much higher than in the case of a wind farm situated only 10 km away from shore. Not to mention that at larger distances away from shore, the negative effect of adverse weather conditions can be significantly amplified, further restricting the access to the wind turbines while increasing the risks for the maintenance crews sent out. This can slow down the O&M work, while also making it more costly. It can also prolong any potential downtime periods, thus leading to further financial losses for the wind farm owners. .

Besides the increased distance from shore, another factor which is expected to exacerbate the effects of poor reliability is the increase of wind turbine rating. Most of the near-shore wind turbines rate at 2-3 MW, but there is a steady trend for

offshore wind turbines to get larger with ratings in the range between 5 and 10 MW and ambitions to reach even higher – towards the 20 MW mark [11]. Thus, a smaller number of installed machines can deliver the same or even larger amounts of power than before. The problem is that the breakdown of a single 6 MW wind turbine is equivalent to the shutting down of two 3 MW or three 2 MW ones, i.e. the larger the turbine, the larger the loss of generation capacity when it goes down.

In summary, the two factors discussed above – i.e. the difficulty of access and the higher turbine ratings leading to larger potential losses from the downtime of a single unit – can have a significant negative effect on the cost of offshore wind O&M. Onshore the cost of the replacement component and the ease of its installation seem to be the primary concern for the O&M operations and therefore the relatively frequent failure rate of inexpensive and easy to repair components (such as the power electronic converter) is tolerated and addressed with reactive servicing (as it can be performed promptly without significant financial or generation time losses). Offshore, however, the cost of a replacement component is often only a secondary concern. The primary concern in this situation is whether or not this component fails frequently and whether or not the consequences of its failure are significant (e.g. causing full shut down of the wind turbine). Thus, faults that have been trivial to fix onshore may become a serious problem offshore. Frequent failures are especially undesirable not only because maintenance trips offshore cost much more than onshore, but also because the weather conditions may significantly delay and restrict the time windows within which such trips can

be carried out. For safety reasons, offshore O&M work is allowed to take place only at wind speeds of less than 10 m/s and wave height of less than 2m. Meteorological data for the North Sea suggests that there could be prolonged periods of time (several weeks or even months during the winter) without suitable time windows for maintenance to take place (from communications with the maintenance provider SeaRoc and offshore wind consultants at ORE Catapult, Blyth). Any delay in maintenance means prolonged downtime which in turn means more losses of potential revenue. Unfortunately, the windy periods – i.e. the best time for peak power generation – tend to coincide with both the time when failures are most likely to occur and the time when access to the wind turbine is most problematic.

To reiterate, although onshore the reactive maintenance routines may be sufficiently cost effective for some low-cost and easy to service wind turbine subassemblies, offshore this is no longer the case. In offshore settings, other factors such as the frequency, the timing and the duration of the wind turbine downtime can have higher impact on the cost of energy than the actual expense of fixing the faulty component. This is due to the much more limited access to offshore sites and the increased rating of the offshore wind turbines. Currently the availability of offshore wind turbines is much lower than that of their onshore counterpart, the cost of offshore wind energy is much higher. If this persists, it may divert investor interest from offshore wind towards other – currently less risky and more lucrative – low carbon technologies. To avoid this, the offshore wind industry needs to adopt different O&M practices from the ones used onshore and improve its technology

reliability with special focus on the relatively frequently failing subassemblies (such as the power electronic converter).

1.3 Converter Reliability Issues

Although wind turbine topologies can vary significantly with respect to the type of generator they use and whether or not they include a gear stage, the variable speed concept is firmly adopted by all modern wind turbines of higher power rating. As such, all offshore wind turbines have variable speed drive trains. Variable speed operation has many advantages, but it also necessitates the use of power electronic converters. With the single exception of a design which is not yet fully commercialised (i.e. the variable ratio hydraulic gearbox with synchronous generator) [12], the generators of variable speed wind turbines cannot be connected directly to the national AC grid. They need a converter to change the frequency of the generator electrical input to the 50 Hz frequency of the grid and to control the flow of power.

At present, all offshore wind turbines include a power electronic converter subassembly and it is safe to say that most of the ones installed in the future will also have it. The converter is the interface which allows the wind turbine's connection to the grid. If this interface experiences a fault or a breakdown, the grid connection will be severed and the export of power will be interrupted. Overall, this will render the whole wind turbine inoperative. It will not be able to generate electricity and feed it into the grid until the converter issue is fixed, which, as

discussed above, can take a considerable amount of time and effort in an offshore setting. Therefore, it is important to take a closer look into the failure rate statistics and reliability issues of the wind turbine power electronic converters.

A paper on wind turbine reliability produced in cooperation between Fraunhofer IWES and Durham university [13] gives an overview of the main existing wind databases: WMEP, LWK, Windstats, VTT, Elforsk, EPRI and NEDO. From their statistical analysis, presented in Figure 1 below, it is obvious that although those databases vary in type and size of the turbine population, monitoring period, failure and subassembly definitions, etc. they all show that the electric system (which includes the power electronic converter) is one of the most frequent sources of failure for the wind turbine.

Data Source	Time Span	No. of Turbines	Highest failure rate		
WMEP	1989 – 2006	1500	1.Electric	2.Control	3.Sensors
LWK	1993 – 2006	241	1.Electric	2.Rotor	3.Control
Windstats	1995 – 2004	4285	1.Rotor	2.Electric	3.Sensors
Windstats	1994 – 2003	904	1.Control	2.Rotor	3.Yaw-System
VTT	2000 – 2004	92	1.Hydraulic	2.Rotor	3.Gearbox
Elforsk	2000 – 2004	723	1.Electric	2.Hydraulic	3.Sensors
EPRI	1986 – 1987	290	1.Sensors	2.Electric	3.Control
NEDO	2004 – 2005	139	1.Sensors	2.Control	3.Rotor
Operator A	2000 – 2007	403	1.Control	2.Electric	3.Rotor
Operator B	2002 – 2009	14	1.Sensors	2.Hydraulic	3.Electric
Operator C	2003 – 2008	23	1.Electric	2.Rotor	3.Gearbox

Figure 1. Comparison between different wind reliability databases and operator reports [13]

Other studies and analyses of the available wind reliability data [14]–[17] also confirm that the electrical system shows highest failure rates amongst all wind turbine subassemblies. It must be pointed out that some of the wind turbines considered in these databases (e.g. the older Danish concept fixed speed wind turbines) do not have converters. Thus the studies use the more general term "electric system", rather than referring specifically to the power electronic converter.

However, the more recent ReliaWind project does name the power electronic converter subassembly specifically as one of the main contributors to wind turbine failure rate. This project supports the improvement of wind turbine reliability through developing a quantitative approach towards measuring it. As part of its first work package, a field study was carried out which analysed operation data from variable pitch wind turbines of higher rating from multiple manufacturers. According to the results of this study, the power electronic converter is the second most significant contributor to the overall wind turbine failure rate and downtime after the pitch mechanism. It accounts for about 13% of the normalised wind turbine failure rate and about 18% of the downtime [6], [18], [19]. This is shown in the figures below (from the quoted publications).

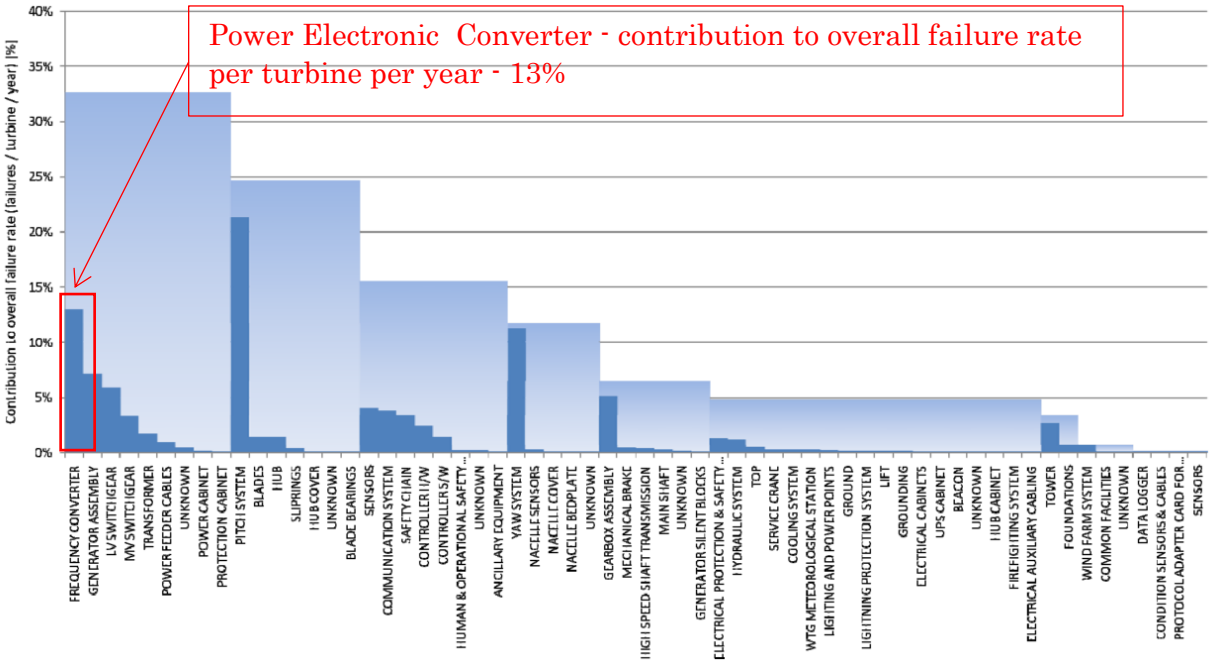


Figure 2. Normalised failure rate contribution of the wind turbine subassemblies [6].

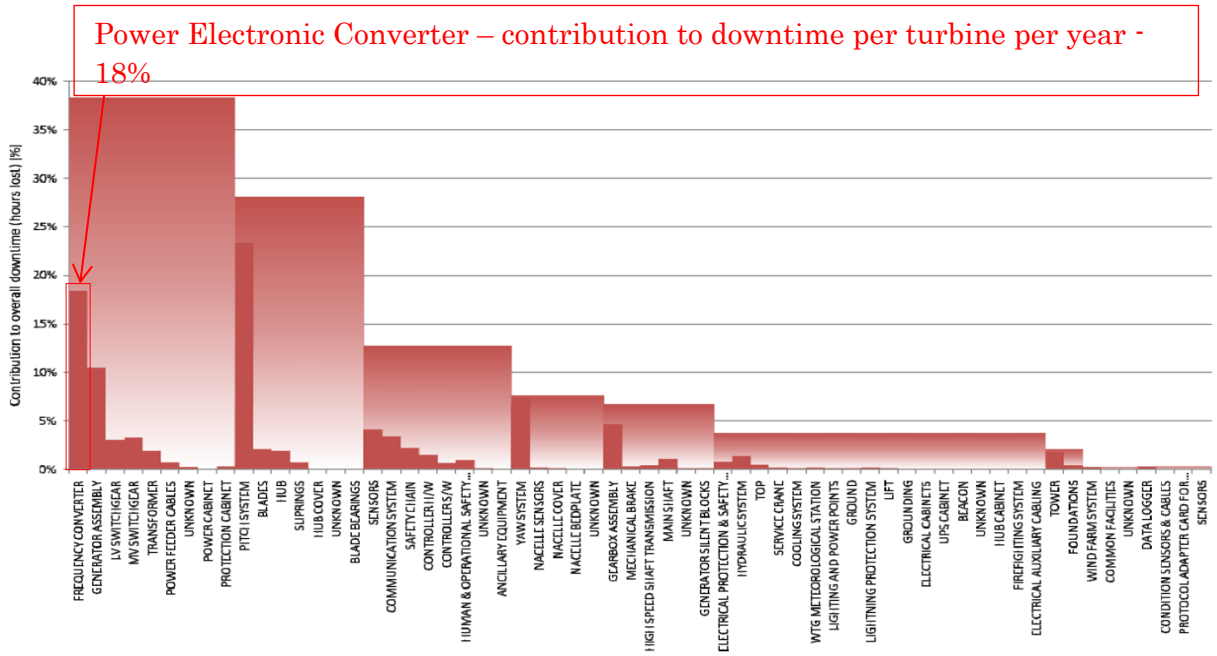


Figure 3 Normalised downtime contribution of the wind turbine subassemblies [6].

This is an onshore study. There are no similar statistics yet for offshore wind and the reasons for this are as follows. Firstly, there are much fewer offshore wind farms and they are overall a much more recent phenomenon, so physically there does not exist the same amount of data about their operation. And secondly, in this yet developing sector, the manufacturers and operators are still unwilling to publically share data (such as failure rates and O&M statistics) that might lead to negative publicity for their products or services. Early on in this project a number of offshore wind farm operators were contacted with requests to supply some O&M data for this academic research, but all refused communication.

Although offshore-specific O&M data is hard to obtain, the technology used in onshore and offshore wind turbines is very similar, especially when it comes to the power electronic converter. Thus, the onshore statistics provide good grounds to assume that its failure rate will remain high in offshore wind turbines. Moreover, it can be expected that the downtime caused by it offshore will be drastically amplified by of the difficulty of access for servicing. So, unless converter reliability is sufficiently improved, it can have a significant negative impact on the availability of offshore wind turbines for electricity generation and thus, on the LCOE of offshore wind.

It is fair to say that the move of the wind industry offshore may prove to be one of the leading factors responsible for the renewed interest and action towards improving the reliability of the power electronic converter and its components.

1.4 Ways of Addressing the Converter Reliability Issues

There are different strategies for improving the reliability of the power electronic converter. They can be divided into the following categories:

- Improving the designed reliability of the converter. This includes improving the designed reliability of the separate converter components such as semiconductor power modules, capacitors, electrical connections, etc. or using the same components, but with improved converter topology. It can also refer to over-rating – i.e. achieving a more reliable overall design by using components of higher current and voltage ratings than the levels expected in normal converter operation, implementing a better cooling system, capable of dissipating much more heat than expected, etc.

- Prognostic approach of calculating the end of the useful life of various converter elements and organising scheduled maintenance to replace them before they fail catastrophically. Component manufacturers often provide lifetime curves for their devices and techniques to calculate their expected lifetime. These techniques generally involve cycle counting and damage accumulation. Varying loading is also a factor that should be considered in the remaining lifetime prediction. For this reason, prognosis techniques can prove hard to apply to wind turbine converters – because of the unpredictability of their generator mission profiles (which is weather dependent and hard to estimate long term). Aside from

this, the most popular ones using linear damage accumulation methods, may predict longer than actual component lifetimes. Attempts have been made to achieve better lifetime prognosis [20], [21].

- Adding in-built redundancy. This can also be described as a specific case of improving the system's designed reliability. For components expected to fail more frequently, redundant counterparts are included, so that when a working component does fail, its function will be automatically transferred to its (until then idle) double ensuring uninterrupted operation. Although it cannot be used for mechanical components such as blades, it is highly applicable for electrical circuits and therefore can be used in wind turbine power electronic converters - an example is discussed in [22]. Including multiple levels of redundancy can indeed prevent failure over a given period of time. It has been successfully used in a number of critical applications (e.g. in the aviation industry) However, it is questionable whether this is best way forward for offshore wind converters, as redundancy can only delay converter breakdown and it does not prevent the need for reactive maintenance. Simply adding more redundant components is not a smart way to go, as it will increase the cost and bulk of the converter without optimising its design. The main problem with relying on only on in-built redundancy is that if the original component fails the operators may not become aware of this, as the redundant component will simply take on its function. They may be lulled into sense of false security and fail to schedule essential preventative maintenance before the redundant device fail. There is no sure guarantee how much time of

uninterrupted system operation the redundant device (or devices) will buy. Therefore, redundancy by itself will not address effectively the converter reliability issues in offshore wind turbines. For such systems it is far more beneficial to have remote visibility as offered by the next strategy for improving converter reliability.

- Condition or health monitoring. This is process of keeping track of the state of health of a given component/system through supervisory data acquisition and early detection of failure mechanism's initial stages. For effective condition monitoring a set of sensitive parameters has to be identified whose change outside given limits will signify in consecutive order the beginning of their deterioration, their degradation in process and end of life. Condition monitoring employs prognostic and diagnostic techniques, but there is a difference between prognosis, diagnosis and condition monitoring in terms of how each views failure. Prognostic approaches to lifetime estimation are interested in the probability of the failure cause and the respective time of the failure effect. Diagnostic approaches focus on the failure mode trying to identify the nature of the problem or the failure cause. Condition monitoring techniques are interested in the whole process of failure cause, development and effect, but its predominant focus is the failure mechanism [23], [24]. Condition monitoring is the only one of the means discussed so far which allows remote visibility over the state of the system and/or its components. Remote visibility is the cornerstone of remote control. By using remote control offshore the operators can act far more quickly and cost effectively to avoid catastrophic failure (e.g. by de-rating or shutting down the system) than reactive maintenance as it is

done onshore. Condition monitoring can also be an invaluable tool optimising existing routine maintenance practices by planning in advance and scheduling maintenance according to the need for it and the weather conditions.

It is important to note that all strategies of improving the reliability of power electronic converters in offshore wind applications are important and the best outcome can be expected, if all are pursued in parallel. However, as no design is 100% fault proof and as no prognosis can claim 100% accuracy, the focus this research project is specifically upon condition monitoring for power electronics, which apart from being a novel concept itself and still in its infancy stages of development, is also the only strategy that aims to provide visibility over the operation of the remote offshore equipment. Developing means for such remote visibility can help improve significantly both the designed reliability of the power electronic converters and the strategies for their operation and maintenance. It is also necessary to allow remote control of the system which may further optimise the power electronic components useful life and the availability of offshore wind turbines.

1.5 Condition Monitoring Potential Benefits

The use of other condition monitoring systems for wind turbine subassemblies such as the gearbox and rotor has become the regular industry practice. They can be integrated with the SCADA interface as part of the wind

turbine full control package. Some of the best known providers of condition monitoring solutions are companies like GL Garrad Hassan, Mita Teknik and Bachmann [5], [25]. Condition monitoring does add of bit of extra cost and complexity to the wind turbine control system, but it has proved that its benefits far outweigh the disadvantages [26].

Taking into account factors such as the probability of the occurrence of converter failures and statistic wind distribution in the year a study on the benefits of condition monitoring [27], [28] presents an evaluation for a 2 MW offshore wind turbine unit. It concludes that condition monitoring for the full turbine – including a potential condition monitoring system for the converter subassembly – would result in an annual saving over £70k, which more than the cost of the average cost of an offshore wind turbine controller as given by [25]. Another study based on failure simulation tool for optimising offshore wind farms maintenance strategy also confirms that informed O&M based on visibility and event predictability provides more cost and time effective solution than purely reactive maintenance [29].

Although the area of condition monitoring for power electronics attracts considerable interest at the moment, there are still no commercially available power electronics condition monitoring systems for the offshore wind market and no information has yet been found about any systems under trial. And although power electronic converters are used in a range of other applications, there is as yet little headway in the area of their condition monitoring. (There is only one known

system (Amantys) for traction applications – currently still in trial – aiming to optimise the operation of the Portuguese railways by tracking IGBT loading and health status using gate driver signals [30].)

It is understandable that before industry makes any serious attempts at the development of such systems, the manufacturers and operators would be interested to the potential value of power electronics condition monitoring as well as its associated extra cost and limitations. As pointed out above, the main justification for power electronics condition monitoring in offshore wind turbines, as opposed to onshore where reactive maintenance is sufficiently cost effective, lies in the fact that while converters are a frequent source of failure the access for their servicing can be problematic. This means that faults may take very long time to rectify and the resulting forced downtimes can cost the operators a large loss of potential revenue. If in such case a condition monitoring were used, its capability to keep track of the system's (or specific component's) health and communicate it to the operator, would mean that they would have a much longer warning time before failure could cause shutdown and therefore a much longer window to plan and take action. Thus, shutdown can be altogether avoided.

Here, a straightforward example calculation is attempted focusing on the financial losses associated with the downtime costs for an average 5 MW offshore turbine. It can be used to illustrate the point that the value of power electronics condition monitoring in an offshore wind turbine can greatly outweigh the added cost of having such a system in place. (This was also published in [11].)

UK offshore wind farms have reported capacity factors as high as 50% for the new higher rating offshore wind turbines – this is mostly due to the fact that the offshore locations have much better wind resource than onshore. We shall use this ballpark figure to calculate the indicative amount of energy the turbine is expected to generate per day is:

5 MW x 24 hours x 0.5 = 60 MWh

The average base level price for energy from offshore is about £30 per MWh, but including the double ROCs (2 times, around £60) [39] it becomes around £150 per MWh in total. We shall use the more conservative figure of £140 (including ROCs) as the current buying price per MWh from offshore wind, as suggested by a private offshore wind development consultant:

£140/MWh x 60 MWh = £8,400

This can represent the average loss of revenue per day that could have potentially been delivered by the 5 MW turbine, if it was operating.

O&M companies typically charge £5k-£6k for a vessel with 2-3 people crew to be sent out on a maintenance trip (from communications with offshore maintenance provider SeaRoc and offshore wind consultants at ORE Catapult). This is expensive in comparison with onshore maintenance, but nevertheless it can be seen that even a single day of unscheduled downtime costs more than that, so it will be in the operator's interest to restart generation as soon as possible, even if it costs them £5k-£6k go get a boat out. The fact that there is no visibility over what

may have caused the failure and which components may need replacing is likely to incur more than one maintenance trip.

The reported average downtime associated with power electronic failures onshore is fairly short – about 1 day per fault. Offshore, however, access to site highly depends on the weather condition

For the sake of our calculation, we shall use a conservative figure of 5 days between the time of the converter failure causing full turbine shutdown and the time when the turbine goes live again. That this is a reasonable and even optimistic assumption for an average offshore servicing time delay as it has to include: 1) the remote diagnostics associated with the fault, 2) securing the spare parts and the qualified staff to fix them, and 3) organising the logistics of the servicing trip.

5 days x £8,400 downtime losses per day = £42,000

The longer the forced downtime, the higher the revenue loss will be:

£42,000 + £5,000 (cost of servicing) = £47,000

Just for comparison, the average total cost of a wind turbine controller including certain condition monitoring capabilities as offered by companies such as Bachmann and Mita Teknik costs only about £70,000 [25]. If over its lifetime of 25 years the turbine experiences only two converter failures they will already have cost in downtime more than the capital cost of the entire electronics control equipment. If the turbine experiences only six or seven such downtimes caused by

the converter, their total cost will outweigh the capital cost for the entire power electronic converter, not to mention the fact that each time a converter module fails, the new replacement itself will cost a portion of the converter price.

Consider the scenario where every wind turbine in a farm of 100 MW wind farm (20 x 5 MW turbines) experiences a power electronics failure once in 2 years (a reasonable assumption as the WMEP database points to 1.5 electrical/electronics failures per turbine per year) with associated downtime conservatively estimated as only 5 days per individual failure. The resultant financial loss is close to a half a million pounds per year:

(20 turbines x £47,000(5-day downtime + O&M cost)/2 years = £470,000 downtime costs per year

And even, if this failure rate is reduced in the modern offshore wind turbines to one third of the quoted-above figure, it can still mean great financial loss over the lifetime of the wind farm and very high associated risk factor for potential investors.

Now, let us consider the cost of a possible condition monitoring system for power electronic devices. The proposed converter level model-based approach will need the sensing of different temperatures as well as current and voltage measurements which are already being used in the controller. Some of the power modules come with incorporated temperature sensors and it is possible that their signatures are already being data-logged and used by the controller or the wind

turbine's SCADA (supervisory control and data acquisition) system to schedule maintenance and/or modify the operation of the converter. Existing capabilities need to be thoroughly examined, but on average for hardware the additional costs of the condition monitoring system will only be associated with perhaps 6-12 new temperature sensors, expected to cost less than £1,000 per turbine including retrofitting and calibration. The signal processing, data management and communication and system licencing costs are expected to be a bit higher than that, but probably within the range of £3k-£4k per turbine.

It is true that there are risks associated with condition monitoring related to how accurately it works and the fact that it adds cost and complexity to the wind turbine system (i.e. another bit that could go wrong). But looking at the above average downtime cost and the relatively low cost of such a potential condition monitoring system, it is clear that even if it manages to prevent a single relatively short forced shutdown for the offshore turbine, it would have paid back for its cost. And as the unit capacity of the wind turbine increases, the relative cost of power electronic condition monitoring will become even lower and its cost saving value even higher.

So the answer to the question whether power electronics condition monitoring will be valuable and whether it is worthwhile the efforts to develop it, is definitely yes. The following chapter looks into earlier work on this subject.

Chapter

2 Research Background

2.1 EPSRC Project COMPERE

The work documented by this thesis originated as a KTP (knowledge transfer partnership) project between the University of Warwick and Narec (subsequently the ORE Catapult). This project itself was a direct descendant of the EPSRC project COMPERE (Condition Monitoring Power Electronics for Reliability). COMPERE was led by a joint academic research team from the universities of Warwick and Durham in cooperation with a number of industrial partners [31]. Its goal was to investigate the feasibility of power electronics condition monitoring for industrial applications and suggest possible ways this can be achieved on-line and without interruption of normal operation.

2.1.1 Industry survey of converter components' failure rate

An important part of the COMPERE project work was the carrying out an industry-based survey to find out which power electronic components are reported as the most common source of converter failure [32]. According to this survey, the semiconductor devices account for the highest percentage of failures, followed by the capacitors in second place. These findings are illustrated by the figure below published with the survey results.

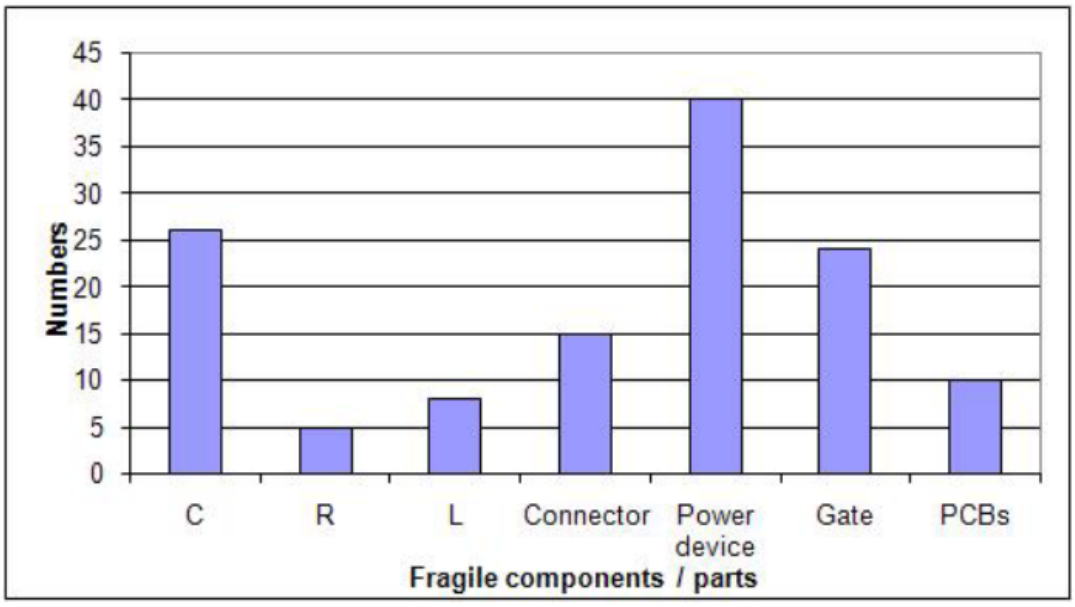


Figure 4. Converter components most susceptible to failure. [32]

The context of the wind industry itself also provides evidence for the high failure rate of the semiconductor devices. According to the WMEP database, half of

the wind turbine converter failures are caused by damage of the semiconductor switches [13]. Further on in the course of the current project we established direct communications with the Siemens Wind Power converter design team who also confirmed that the most frequent source of failure in their converters were the IGBT modules.

The industry-based survey by COMPERE reports the capacitors as the second most common source of failure. However, in the recent years they have seen some well commercialised design improvements. Thin film capacitors with much higher ripple current capability and life expectancy are quickly replacing the older electrolytic technology. Apart from that, some reliable on-line condition monitoring techniques for capacitors have already been developed based on measurement of their capacitance and equivalent series resistance (ESR) [33]–[35]. Therefore, the current PhD project does not go into the direction of capacitor reliability, but focuses more narrowly on the semiconductor devices.

2.1.2 Power electronic condition monitoring prior to COMPERE

Another significant output of the COMPERE project is their comprehensive review of power electronics condition monitoring which includes a discussion of all known to-date condition monitoring techniques for semiconductor devices (e.g. IGBT modules) [36]. This work was based on thorough literature reviews of a

number of earlier research projects and publications focused on power electronics reliability [23], [37].

The existing techniques for condition monitoring of IGBT power modules reviewed by COMPERE can be classified into the following categories:

1. **Technique based on measuring the on-state voltage (V_{CE}) or resistance (R_{ON}) for bond wire lift-off detection.** This method is rather difficult to achieve for real time measurements with guaranteed accuracy because of the relatively small value of the on-state voltage on the background of the dramatic switching transient and the changes due to different current levels. The physical dimension, isolation, cost and integration of the sensing circuits within the power module also pose difficulties for the practical implementation of this system. The on-state voltage measurement has been proposed as quasi real-time failure prognostic method in an electric vehicle application where the on-state voltage was measured only at cold start-up with known starting current and temperature [38].

2. **Thermal resistance and temperature measurement based condition monitoring.** As discussed above the power losses naturally occurring during the semiconductor device operation are dissipated as heat which in the process of repeated cycles can damage the chip and its packaging. Each of the layers of the IGBT module has its thermal impedance (thermal resistance and thermal capacitance) which obstructs the heat flow. As the creep fatigue damages the bonding materials over time, the thermal resistance is increased and the internal

chip temperature gets higher and higher. Therefore another parameter very important for determining the health of a semiconductor device is its junction temperature – T_j. Most IGBT devices are designed to operate at rated junction temperature of 125°C and maximum junction temperature of 150°C [39]. T_j is highly valid for condition monitoring, but its direct sensing is currently impossible in practical applications. It must be estimated using other parameters. [40] suggests a technique that relies on the nearly linear relationship between V_{CE} and T_j at low current (100mA). Other thermosensitive parameters for which condition monitoring techniques have been attempted in lab conditions are the threshold gate voltage V_{GE}, and the transconductance of the IGBT derived from the dI_C/dt and dV_{GE}/dt. This method has been suggested as suitable for on-line application, but it was found to be affected by noise and by the presence of temperature compensated gate resistors used in some IGBTs. Some direct sensing methods have also been tried including the use of infrared cameras and even X-ray for crack detection. Those two methods, however, are not deemed practicable for large scale on-line applications.

3. **Switch-time-based condition monitoring for the power device and its gate driver.** Another parameter which can be used to signify the presence of several failure mechanisms is the increase of the switching time. The advantage of this method is that it uses the gate driver signals of each individual device and thus offers noise immune means of condition monitoring. It has been applied in GTO systems (which have long switching times of the order of 10μs) [41]. However for

MOSFET or IGBT converters where the switching time is in the range of 100-500ns, this method is still not deemed practical. This method however may further be developed using indirect techniques of switch-time measurements such as the high frequency electromagnetic interference signal change[42], [43].

4. **Gate-signal-based condition monitoring for gate degradation.** A method based on the waveform of the gate voltage during turn ON is suggested for detecting short circuit IGBT faults [44]. Experiments indicate there is a marked difference in the level and duration of the Miller gate plateau in the case of the healthy and the faulty devices. This method is not yet developed for condition monitoring, the limitation being that very high sampling resolution is necessary for the measurements to capture and plot the Miller Plateau, therefore other ways are considered such as using analogue electronics to obtain cumulative charge signature which can be applicable for condition monitoring in converters where immediate shut-down is not necessary.

5. **In-situ or sensor-based condition monitoring.** Sensor-based condition monitoring relies on use of additional circuit elements to detect signatures of degradation that such as the increase of voltage drop, for example. An early technique suggest use of a resistor in parallel to the emitter bond-wires for their lift-off detection [45]. The IGBT module manufacturer SEMIKRON presented a method for condition monitoring using sensor integrated in the DBC of an intelligent power module to monitor the change of resistance resulting from wire bond lift-off [46]. Earlier attempts Those methods produce very good results.

However, they necessitate direct access to the chip and changes of the power module design. As such, they are open only to device manufactures to start producing condition monitoring enabled semiconductor modules, and not for retrofitting condition monitoring functionality to a wider range of power electronic devices currently in operation and on the market.

6. **System-identification-based condition monitoring.** As the degradation of a power device usually affects the converter as a whole and in theory changes identified on system level can be used for condition monitoring as well. For example, monitoring technique for the health condition of output filter capacitors has been reported using the shift of frequency response [47]. Potentially other parametric variations available on system level can be used to provide early warning for developing faults [48]. Development of neural networks may provide the answer to power electronics condition monitoring. Such a network has been applied to a diode and was able to detect most relevant component changes [49]. System based condition monitoring for power electronics is still underdeveloped though, and dependant on factors like establishing unambiguous correlations between specific failure modes and the system response, advanced processing algorithms and increased demand on the computing hardware and attenuation of high frequency noise.

Table 1. summarises the above condition monitoring categories with their advantages and disadvantages. At the time of publication none of these techniques had been tested outside a lab setting or successfully deployed in industrial

applications. Therefore, none of them has been confirmed as suitable for in-operation online condition monitoring. However, as the COMPERE review paper points out, the whole field of power electronics condition monitoring is still in its infant stage of development and that the techniques explored so far may still be subject to continuing intensive development.

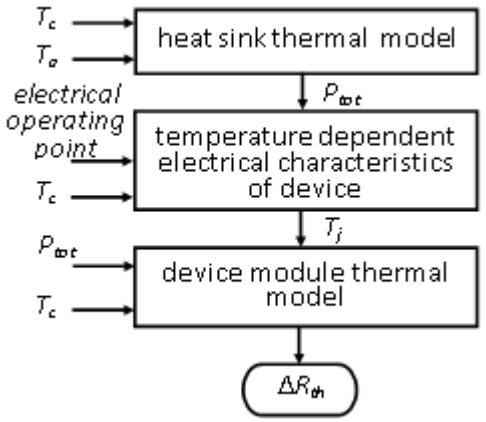
Table 1. Techniques suggested for condition monitoring of power electronic modules prior to the COMPERE project.

Condition Monitoring Means	*PRO's*	*CON's*
V_{CE}(on), R_{on}	High relevance for detection of degradation of both solder layer and bond wires.	Difficult to measure small on-state V_{CE} changes on background of large voltage differences.
R_{th} (thermal resistance)	Identifying solder fatigue.	Difficult to measure T_j in operation.
Gate voltage waveform	Identifying electrical faults.	High real-time requirement.
Prolonged switch-time	Identifying gate drive failures.	Difficult to measure ns-range switching times.
Embedded sensors	Reliable and accurate.	DBC modification is necessary; expensive custom-made modules must be used.
System-level identification	No additional hardware required.	Difficult to correlated faults with system symptoms; complicated algorithms needed.

2.1.3 New condition monitoring methods with potential for on-line application identified by COMPERE

The COMPERE project also investigated new possible methods for power electronics condition monitoring which can be developed into on-line industrially applicable solutions. Three such methods with the potential for on-line operation were identified and published as part of the COMPERE project:

1. A new temperature based approach using changes in the temperature difference between the power module case and ambient air ($\Delta T_{c\text{-}a}=T_c - T_a$), to detect changes in the R_{th} of the module and thus monitor its solder fatigue [50]. The $\Delta T_{c\text{-}a}$ – unlike T_j – can be easily obtained from external temperature measurements of the power module and heat sink during the normal operation. This study suggests that since the electrical power loss of the module is dissipated as heat through the heat sink, then from the case and ambient temperatures using an appropriate heat sink thermal model the total power loss of the module can be computed. Using the converter operating point parameters (i.e. current, duty ratio, etc.) and the case temperature, the total power loss already estimated can be matched to a corresponding T_j value at which it should have occurred. Then, the T_j, total power loss, T_c and a nominal R_{th} value that corresponds to the healthy state can be used to derive a difference in the R_{th} signifying the degree of solder layer degradation. Figure 5 below illustrates this algorithm for extracting the change of thermal resistance.



$$\Delta R_{th} = \frac{T_j - T_c}{P_{tot}} - R_{th0}$$

Figure 5. Temperature-based condition monitoring algorithm proposed by COMPERE [50].

This method was experimentally tested over a range of converter operating points (i.e. – with different output currents and case temperatures), demonstrating that it is possible to extract dynamically the change of the internal thermal resistance as the module ages.

2. An approach using inverter harmonic identification to monitor solder fatigue [51]. It is shown that low-order harmonics, caused by non-ideal switching, are affected by the device junction temperature, which in turn depends upon module solder condition. This can be used to schedule converter maintenance and reduce damage. A change of up to 5.5% of the fifth harmonic due to solder fatigue has been confirmed by simulation and experiment, to be caused by the delayed IGBT turn-off at higher junction temperatures resulting from increased thermal resistance (emulated). Controlled harmonic resonance can be introduced in the inverter to amplify the small signal change. It was suggested that the compensation voltage produced by the control loop can be used as the condition

monitoring signal. This technique has been demonstrated under fixed operating condition and again it faces the challenge to prove itself at variable operating point conditions.

3. Utilising the discovered dependence between the rate of change of the IGBT's on-state voltage during turn-off (dV_{CE}/dt) and its junction temperature (T_j) as a potential means to monitor the IGBT module's degradation [52]. In effect, this dependence represents a new way of estimating the device's T_j in operation. It is suggested that dV_{CE}/dt can be obtained either from direct measurements, or deduced from the low order harmonics that need to be compensated in the control loop. The laboratory experiment curves confirm the dependence: the dV_{CE}/dt drops almost linearly as the T_j increases. Although it may be challenging to derive a complete algorithm measuring and using this dependence for condition monitoring of the IGBT module, this finding is still an important contribution to the list of signatures potentially associated with degradation.

Out of these three methods identified by COMPERE as suitable for on-line condition monitoring, the first one is considered to have the highest readiness level for potential industrial application for the following reasons. Firstly, its test on a lab converter as described in [50] demonstrated that it can detect emulated R_{th} (thermal resistance) increase of the module under test. Secondly, it relies on sensing temperature signals external to the module, avoiding the need for power module modification and integration of complicated sensing circuitry and allowing for the possibility to be retrofitted to any existing converter. Thirdly, it uses

inexpensive off-the-shelf temperature sensors and DAQ equipment; moreover, since thermal signals do not require high sampling rates, the data logging and data processing arrangements will also be simple and straight-forward. Overall, in industry money matters and industry is conservative (i.e. it sticks to tried and tested designs and opposes fast changes) and since the discussed method is not likely to add significant cost to the converter and does not require design changes, but promises easy retrofitting, it seems the most likely candidate to be further investigated for industrial application.

However, this method may need further modification and verification. One of its limitations is that the thermal modelling it uses may not be suitable for power modules of large dimensions or for a heat sink cooling multiple modules. Another limitation concerns the extraction of the thermal model parameters which is difficult to achieve in practice. It is also possible that at elevated junction temperatures, the paths of heat dissipation may change and become more complicated (e.g. instead of all the heat exiting straight-forwardly through the back or baseplate of the module in the direction of the heat sink, some of it may also go along the cables, or start spreading laterally, etc.) It also needs to be verified that this method will work well with liquid-cooled heat sinks, in which case it may need to be re-defined (e.g. by using other temperature than that of the ambient air, etc.)

Since the current research project was conceived as a direct descendent of COMPERE with the idea to use some of its findings and continue its work towards bringing power electronics condition monitoring closer to industrial deployment, it

was decided early on in the project to focus primarily on this first condition monitoring concept. The COMPERE method will not be used in its original form, but we shall take the idea to use external (to the module) temperature measurements combined with operating point information as health-state signatures and propose a field-deployable condition monitoring solution.

2.2 Other Recent Research in the Field

Another project investigating power electronics condition monitoring from roughly the same time period as COMPERE is the German based CoMoLeFo (Condition Monitoring for Power Electronics in Photovoltaic Inverters) lead by Fraunhofer IZM, Berlin. They also focus predominantly on IGBT modules and report developing a condition monitoring system using in-situ life cycle logic units (LCUs) with sensors directly measuring parameters such as the chip temperature, etc. and using rainflow analysis to make predictions about the units remaining lifetime [53]. Fraunhofer researchers have also reported another in-situ technique using of dummy chips as lifetime indicators [54].

As mentioned earlier, the only industry deployed system known so far that has the capability for IGBT condition monitoring is the Amantys system which is being trialled by the Portuguese Railways. Amantys have developed an intelligent gate drive solution which allows the estimation of IGBT and diode junction temperature (with accuracy of ± 5 °C) and measurement of on-state voltage and

collector current. This gate drive technology used in conjunction with their Amantys Power Insight software platform allows on-line monitoring and control of power switching in medium and high voltage applications [30].However, as mentioned earlier, this system was developed for the primary purpose of control, not for condition monitoring per se.

More recently, two other PhD projects held respectively at the universities of Aalborg (Denmark) and Nottingham (UK) published their own proposed solutions for on-line and in-operation condition monitoring of power modules.

The first one proposes a condition monitoring method using the on-state voltage [55], [56]. Although the on-state voltage has already been established as one of the most relevant parameters for detecting degradation inside the module, it has been a challenge to measure it so far with sufficient accuracy for practical health monitoring. In switching applications, the collector-emitter voltage changes dramatically between its ON and OFF states while the on-state voltage rise that needs to be measured in order to detect solder fatigue is very small – typically about 3-5%. The new method proposed for measuring the on-state voltage uses high voltage, low current diodes D_1 and D_2, of as close as possible characteristics to block the high voltage in the power circuit during the off-state from getting into the instrumentation circuit – as shown in Figure 6 for one converter leg [56] . When the IGBT is on, the output of the Op-Amp will be $v_{ce}' \simeq v_{ce}$ as long as the voltage drops across D_1 and D_2 due to the small current I_s are the same.

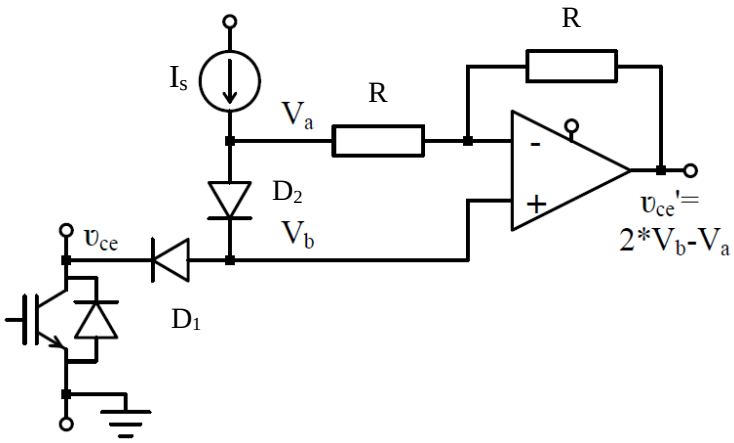


Figure 6. Circuit for sensing on-state voltage[56]

Therefore sampling v_{ce}' in synchronisation with the on-state of the IGBT will show the temperature sensitive on-state voltage of the IGBT, which depends on the current of the converter as shown in Figure 7 from [55].

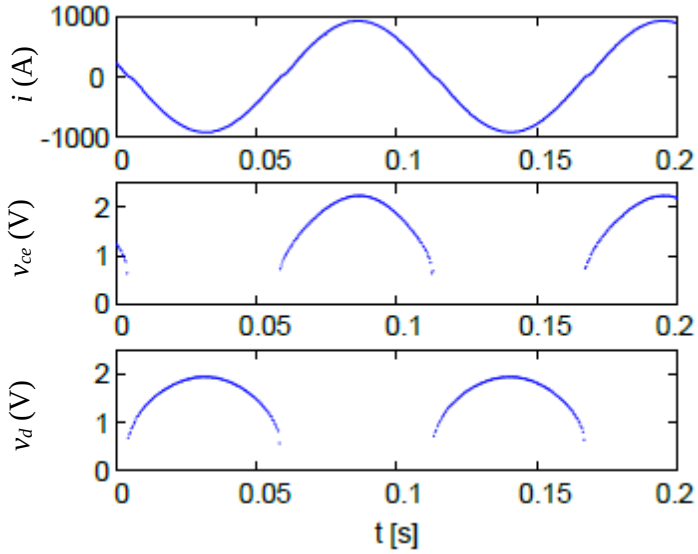


Figure 7. Result of on-state voltage measurement [55]

The second research project [57], [58] proposes a combined approach for in-service monitoring of solder fatigue and bond wire lift-off illustrated by Figure 8 below (form [58]). This method introduces two separate techniques for monitoring solder fatigue (R_{th} increase) and bond wire lift-off (increase of the electrical on-state resistance) respectively. Both of them compare on-line measurements with pre-determined models for the power module in its original healthy state.

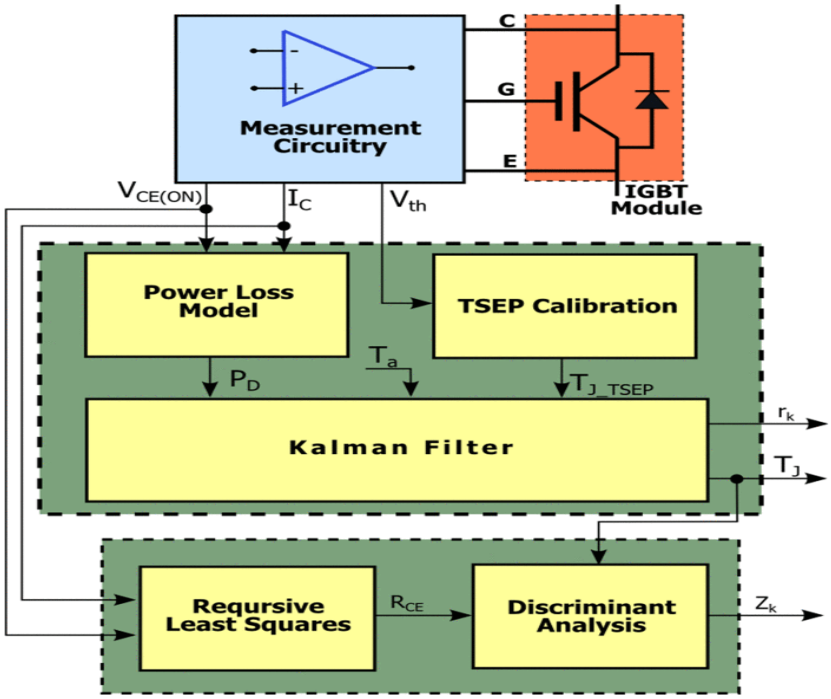


Figure 8. Method for in-service detection of IGBT module packaging degradation [58]

The first technique uses the residual error obtained from a Kalman filter based algorithm which estimates a T_j value from the ambient temperature and power loss look-up tables and compares it to a true T_j value measured via a

temperature sensitive electrical parameter (TSEP) – the gate threshold voltage $V_{G(th)}$. The second uses a recursive least squares algorithm to estimate the electrical resistance from online measurements of $V_{CE}(ON)$ and I_C and since the thus estimated value is also dependant on the T_j, discriminant analysis is applied to it to produce a linear transformation Z_k which is unaffected by the changes in the Tj and reveals only the changes in the electrical on-state resistance caused by the bond wire lift-off.

Apart from projects focusing directly on the power module's condition/health monitoring, another research direction also relevant to the background of this study follows prognostic approaches. This direction has been traditionally of interest to manufacturers as they need to provide some kind of lifetime estimate for their products. They usually do power cycling tests on their devices and based on them publish lifetime curves that can be used for estimating the device lifetime according to its specific cyclic loading [39], [59]–[61]. However, the correct estimation of the device's lifetime is not a straight forward process – especially in applications such as wind power generation where the mission profiles are highly unpredictable. Moreover, the traditional lifetime estimation methods using cycle counting and linear damage accumulation have been found to significantly overestimate the useful life of IGBT modules.

A PhD thesis on this subject [20], published at the University of Warwick, has established that larger swings in the junction temperature ΔT_j at the beginning of the module's lifetime cause much greater damage than the smaller ones. Although

the cycles with small variation of T_j are the majority, the damage caused by them is small in proportion and the early stage consumption of the power module's lifetime is dominated by the effects of the larger temperature cycles. However, as the module ages the difference in the amount of damage caused by larger and by smaller ΔT_j gradually decreases. This means that when the accumulated damage of the power device is in its more advanced stages, the linear methods for calculating its further spread are no longer accurate. The thesis shows, based on power cycling experiments and modelling, that although the traditional use of manufacturers' lifetime time curves with traditional damage accumulation methods predicts fairly long useful lives for IGBT modules (in the range of 20-30 years), the irregular loading associated with wind profiles and the fact that the power module damage accumulation follows a non-linear pattern, is likely to result in a much shorter device lifetime (in the range of 3-7 years). This observation seems so be in agreement with the industry survey discussed earlier that power devices tend to fails much earlier than their expected design end-of-life [32].

Another recent PhD research [62] focusing of IGBT life-time estimation confirms that the role of smaller ΔT_j stress cycles in the later stages of power module's life cannot be ignored without incurring a significant error in the estimated remaining life of the device and suggests models for damage accumulation which produce more accurate end-of-life prognosis.

Although the focus of this research is not on prognosis, its significance for industry application of condition monitoring is also recognised here. Condition

monitoring tracks the real-time changes in the health state of a given component, so that if it drifts significantly away from its initial healthy condition appropriate action can be taken (e.g. replacement, de-rating, etc.) to avoid system shutdown due to this component's failure. Integrating some prognostic elements with this condition monitoring process – to provide an estimate of the device's remaining lifetime based on its current health condition – will also advise the operators on how much time they have to take the necessary actions. Such a monitoring system will have a much better practical value for scheduling maintenance and optimising the system operation control.

2.3 IGBT Power Modules and Their Failure Mechanisms

2.3.1 IGBT device overview, operation and power losses

The semiconductor technology used most commonly in the power electronic converters of wind turbines is the IGBT which in anti-parallel with a freewheeling diode forms bi-directional or 4-quadrant switch capable of blocking voltages of both polarities and conducting currents in both directions. Power modules usually contain multiple IGBT and freewheeling diode chips connected in parallel to provide higher current carrying capabilities. Other technologies, such as the IGCT (integrated gate- commutated thyristor) modules developed by ABB and Mitsubishi, have also started to gain ground lately as offshore wind turbine power

ratings are going up and their drives are changing from low to medium voltage [63]–[66]. However, the use of IGBT power modules still dominates the wind industry, and so the focus of this research project will be on IGBT devices.

The IGBT like most other semiconductor power devices is made of a few layers of differently doped silicon forming p-n junctions within the device. A general overview of the IGBT physical chip structure and the way they function can be found in [67]–[69] and in different manufacturers' documentation, manuals and technical notes such as [39]. A typical structure and operation mechanism of an IGBT is shown in Figure 9 below. It shows the differently doped layers of the Si crystal and the path of the electron and hole current flow. (The contacts' and doping layers' thicknesses are not to scale.)

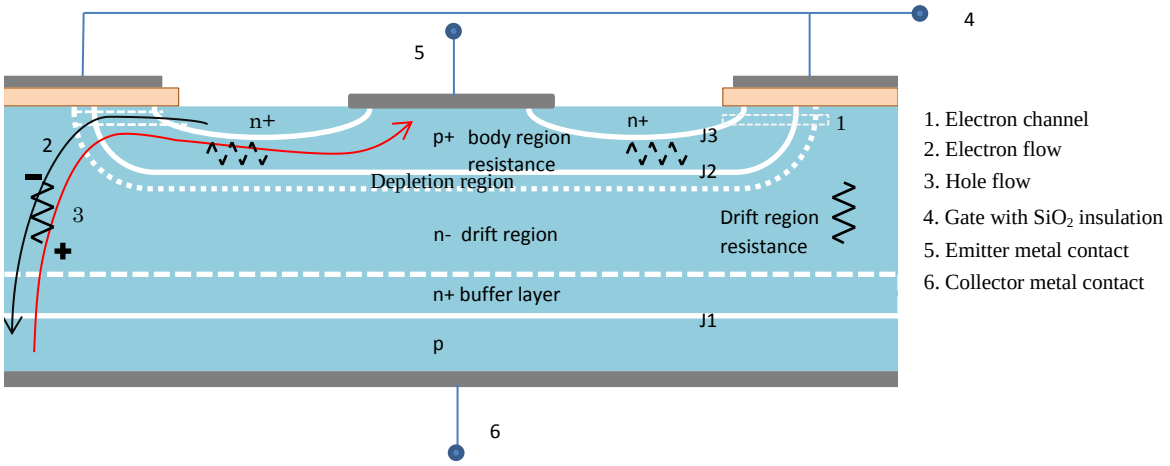


Figure 9. Typical IGBT chip internal structure.

The IGBT goes into a conducting mode when gate terminal is positively biased with respect to the emitter terminal and the gate-to-emitter voltage V_{GE}, often simply referred to as the gate voltage exceeds certain threshold value. The current in the IGBT I_C, also known as the collector current, flows from the collector terminal to the emitter terminal and is comprised of both majority and minority carriers – i.e. electrons and holes respectively. As common in semiconductor devices, the IGBT is subject to a small voltage drop when conducting, known as the collector-emitter voltage V_{CE}. This on-state voltage drop is responsible for the IGBT's **conduction power loss**. It can be expressed as a sum of three components [67], [69] as represented by the IGBT equivalent circuit in Figure 10 a) below:

- The voltage drop across injection junction 1 (J1 in Figure 9 above or the pn junction formed between the p layer at the collector terminal and the n+ buffer or n drift region), which is a typical pn junction drop, exponentially dependent on the current;
- The voltage drop due to the resistance of the n drift region which, too depends on the collector current, but is also on physical properties such as the device active area, carrier mobility and density and the width of the n drift region;
- The voltage drop of the electron channel created under the gate oxide in the p + body layer due to its ohmic resistance, which is also dependent on the physical properties and layout of the device.

There is also a lateral voltage drop component that affects the some of the hole current attracted to follow a path underneath and parallel to the electron

channel in the p body layer. This voltage drop, however, has to be kept to minimum during normal operation to avoid triggering latch-up of IGBT's parasitic thyristor – as shown in Figure 10 b). There are different modifications of the IGBT's internal geometry and doping which have made modern IGBTs essentially latch-up proof [67].

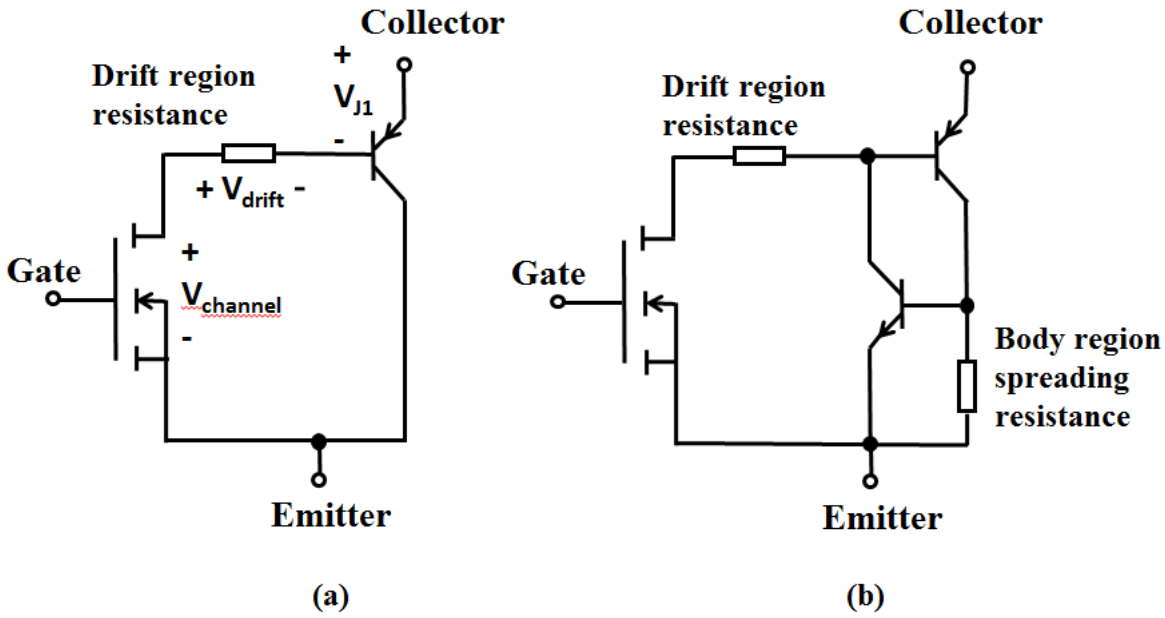


Figure 10. IGBT Equivalent circuits: a) approximate circuit valid for normal conduction; b) circuit showing the transistors comprising the parasitic thyristor and the body region resistance.

IGBT manufacturers normally provide for their devices V_{CE} curves showing its dependence on the I_C for different levels of device internal junction temperature T_j and V_{GE}. These curves can be used to calculate the IGBT conduction power loss.

Apart from the conduction losses, the IGBT also experiences **switching losses** as it turns on and off. Figure 11 below illustrates in detail the stages of the IGBT turn-on process [70].

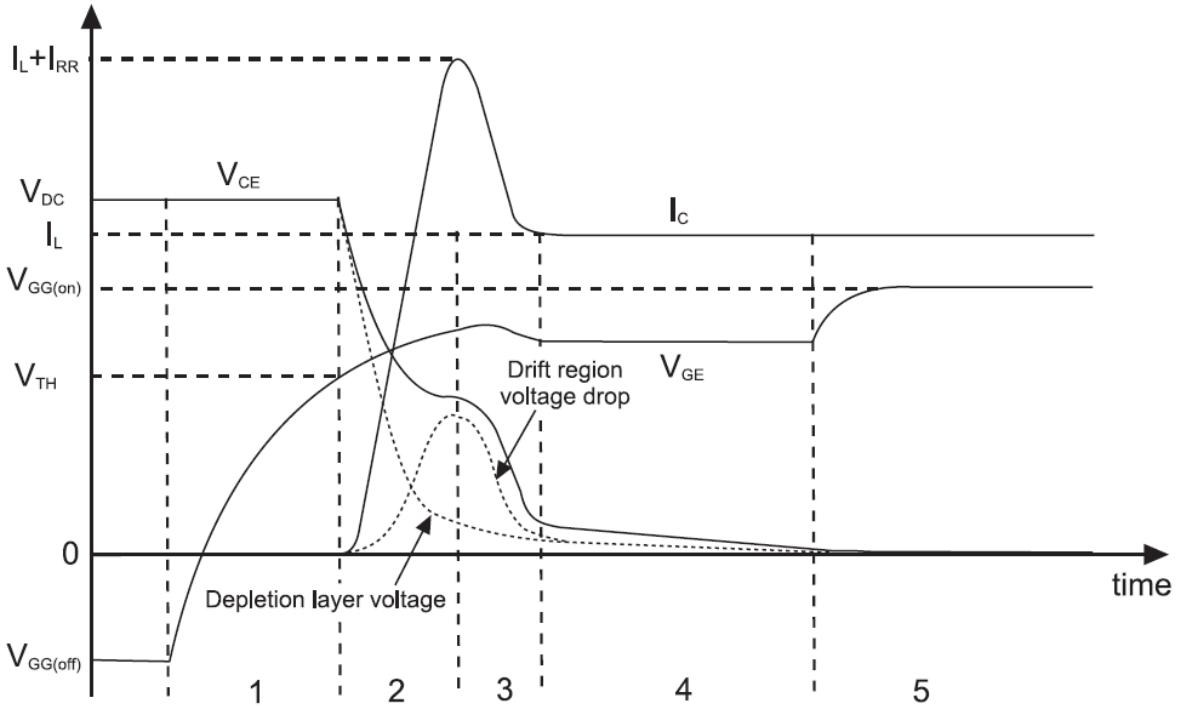


Figure 11. IGBT turn-on process [70].

At turn-on, the V_{GE} starts rising and it the first stage of the process the I_C and V_{CE} are not affected. The beginning of the second stage is marked by V_{GE} reaching its threshold value as it continues to rise, following which an inversion layer (or MOS channel) forms under the gate across the p+ body region (illustrated in Figure 9 above). It allows electrons to flow from the n + layers under the emitter terminal into the lightly doped n-drift region towards the p layer adjacent to the collector

terminal. This in turn stimulates the injection of holes from that p layer into the drift region. The collector current I_C starts rising almost linearly and, as the charge carriers in the drift region increase, the depletion regions shrink back and the voltage drop across the device also begins to decrease significantly. The second stage ends as the I_C reaches its peak above the level of the load current I_L. This overshoot is due to the added reverse recovery current from the diode as it stops conducting. During the third stage the I_C drops down to the level of I_L and the V_{CE} also decreases further as the voltage across the drift region drops downs. The fourth stage is characterised by a plateau in the gate voltage, while the V_{CE} tails off approaching its on-state value. In the fifth stage there is another rise in the V_{GE} until it reaches its final on-state value. The I_C is already stabilised at the level of I_L and the V_{CE} also drops to its on-state value.

The IGBT turn-off also has five stages – as shown in Figure 12 below [70].

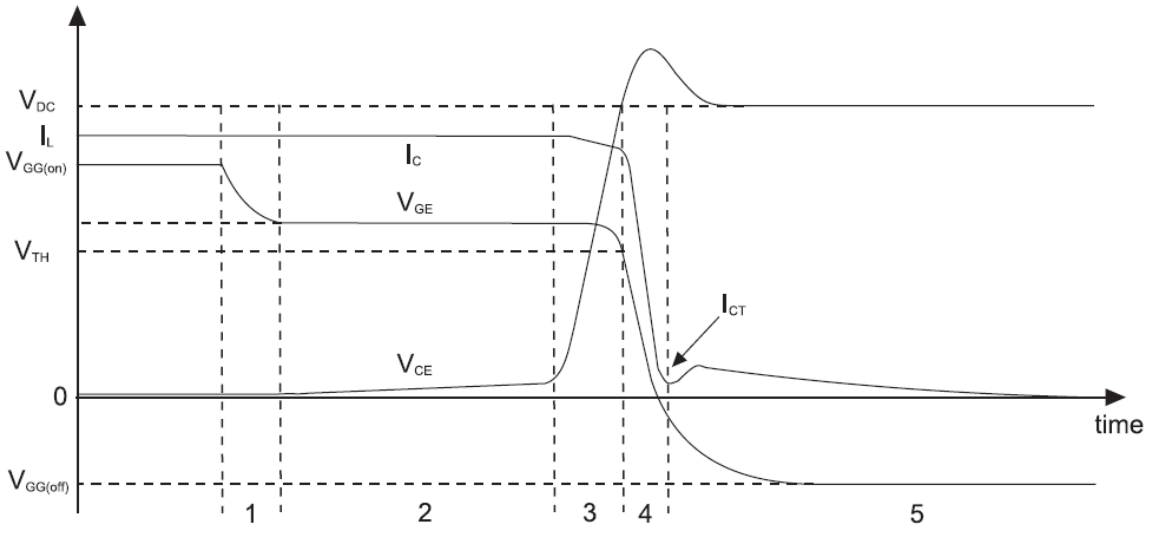


Figure 12. IGBT turn-off process [70].

Stage one of the turn-off is initiated by a small drop in the gate voltage causing discharge of the gate-emitter capacitance and a slight rise in the voltage of the MOS channel and thus also of the V_{CE}, while the I_C remains fixed at the level of I_L. In the second stage the current is still constant as the MOS channel enters into saturation state and the V_{GE} plateaus to support this while the V_{CE} continues to slowly rise. The gate capacitance starts to decrease and the depletion regions expand and start to constrict the path of the current flow. In the third stage the V_{CE} reaches its highest rate of increase while I_C starts dropping as stored charge carriers are being removed from the drift region. V_{GE} exits its plateau level and also starts dropping towards its OFF-state value. During the fourth stage, as the V_{CE} reaches and overshoots the V_{DC}, I_C drops fast, as the current is now diverted

the freewheeling diode. In the fifth stage there is the characteristic for the IGBT slow decay of current tail. This occurs because the depletion regions have reached maximum expansion and I_C is no longer fixed by the I_L, so they cannot continue to swiftly sweep out the few remaining charge carriers in the drift region and those carriers are then being removed, mostly through recombination, at a slower rate. To keep the on-state losses lower, it is in fact beneficial to have longer carrier lifetime, but this will make the current tail decay period longer, and therefore, the turn-off power dissipation – larger. Its duration will also increase with the temperature rise. Therefore, a trade-off must be made between on-state losses and faster turn-off [67].

As can be seen, the turn-on and turn-off processes do not occur instantaneously. It takes some time for the charge carriers to build-up or deplete when the IGBT enters into conducting or blocking mode respectively. During these very small intervals of time (in the sub-microsecond range for the IGBT), there are both voltage across and current flowing through in device – as illustrated by Figure 13 below – resulting in power losses that cannot be ignored.

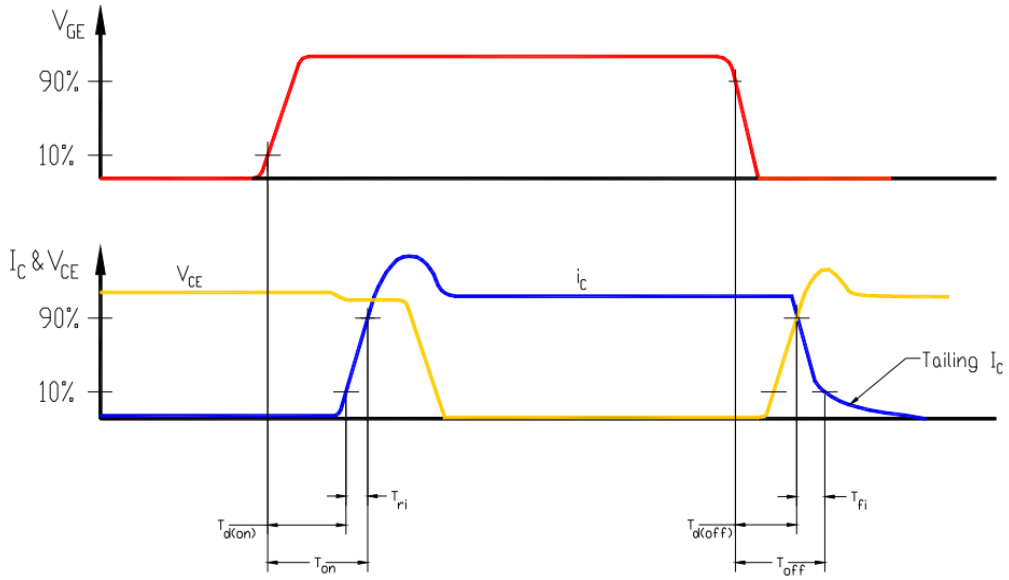


Figure 13. Simplified IGBT switching waveforms illustrating the simultaneous presence of significant current and voltage levels that cause power dissipation [71].

The manufacturers do not normally provide in their datasheets detailed waveforms of the I_C and V_{CE} at turn-on and turn-off, but they do give the typical duration of the switching events (denoted as T_{on} and T_{off} in the figure above) and the delays between the initial change in the gate voltage and initial change in the current signal at turn-on ($T_{d(on)}$) and the voltage signal at turn-off ($T_{d(off)}$) respectively. They also provide information on the switching power losses integrated over time in form of energy pulse at turn-on (E_{ON}) and energy pulse at turn-off (E_{OFF}) which occur once every switching period. The reason the switching losses are given in terms of energy rather than power is that without knowing the device's switching frequency we cannot know how much combined energy it will lose per second. The more E_{ON}/E_{OFF} pulses added up per second pulses, the higher

the power loss. Leaving aside the device design, geometry and doping, the E_{ON} and E_{OFF} losses depend on the I_C, the T_j and the V_{DC}. The manufacturers usually provide a plot of E_{ON} and E_{OFF} against the I_C for at least two different T_j levels and for one V_{DC} level (for practical purposes the dependence of V_{DC} is normally assumed to be linear). These plots and the switching frequency of the device in operation can be used to estimate its switching power losses. More information on IGBT loss calculations is given in [39], [71]–[75]. IGBT power loss calculation and modelling will be discussed further in the next chapter.

It is important to note that the conduction and switching power losses are phenomena that naturally accompany the IGBT's operation – known as power cycling. The device manufacturers try to minimise those losses (by optimising the IGBT geometry, doping, etc.), but they cannot be avoided altogether. The losses manifest as heat generated internally which inevitably causes the IGBT's junction temperature T_j to rise during operation – which also leads to thermal cycling as the device switches on and off. The T_j in its turn affects the device's electrical properties (e.g. carrier mobility, on-state V_{CE}, the duration of the turn-on and turn-off, etc.) resulting in overall increase of the power losses. This is why the T_j needs to be maintained within a safe limit to avoid pushing the device's operation outside of its SOA (safe operating area or the manufacture-defined limits of voltage and current the device can support without self-damage) to preserve the integrity of the IGBT's housing and interfaces via which it connects to the rest of the circuit– i.e. the device packaging which is discussed in the next section.

2.3.2 IGBT device packaging

Semiconductor packaging is an important topic of its own right, as without being appropriately secured in place, connected to the rest of the electrical circuit and protected from the environment and the chip itself has little practical use. The main functions of the IGBT packaging are as follows [39]:

- To allow electrical connection between the chip and the rest of the electrical circuit;
- To allow identification of the component type and its terminals;
- To provide protection to the chip (against moisture, contamination, particles, radiation, structural protection for the fragile semiconductor element, etc.)
- And last but not least, to provide the means of cooling or thermal sink for the heat generated via power dissipation inside the chip.

Although there are single-chip packaged devices available on the market, for higher power industrial applications (such as the converters in wind turbine), multiple semiconductor chips are packaged together in power modules. On the one hand this allows paralleling of multiple chips to achieve higher current carrying capabilities and on the other – it also allows optimisation of the circuit as the semiconductor elements can be assembled in half-bridge converter legs or complete 3-phase converter configurations.

The main two types of power module packages currently on the market are the standard power module with DBC (direct bonded copper) substrate and wire bonds and the press-pack module [20], [24], [39].

A cross-section of a standard power module with DBC substrate is shown in Figure 14. The DBC substrate consists of two copper layers sandwiching a thin ceramic layer which is electrically insulating, but allows heat to escape the module through it. Such modules can come with or without a base plate. Base plates are traditionally added for ruggedness, but can be a cause of concern regarding thermal fatigue of their additional solder layer.

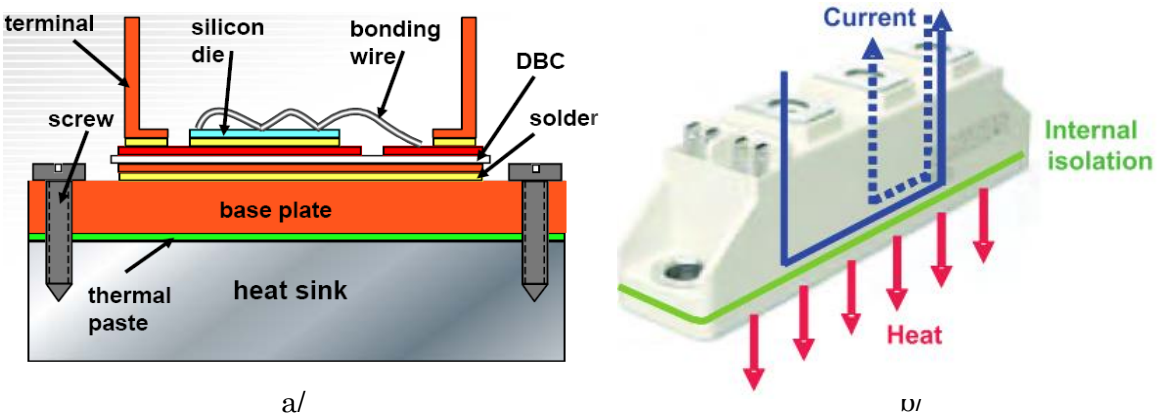


Figure 14. Example of a standard power module: a/ schematic of its internal structure and b/ electrical and heat flow paths out of the module [39].

This type of module can contain multiple IGBT and diode chips soldered collector side (or cathode side – for the diodes) to the top copper layer of the DBC and using bond wires for electrical connection between their emitter side (or diode anode) and module's outer terminals and also between the gate control terminals

and the IGBT gate. Figure 15 below shows an image of an open DCB & bond-wire module.

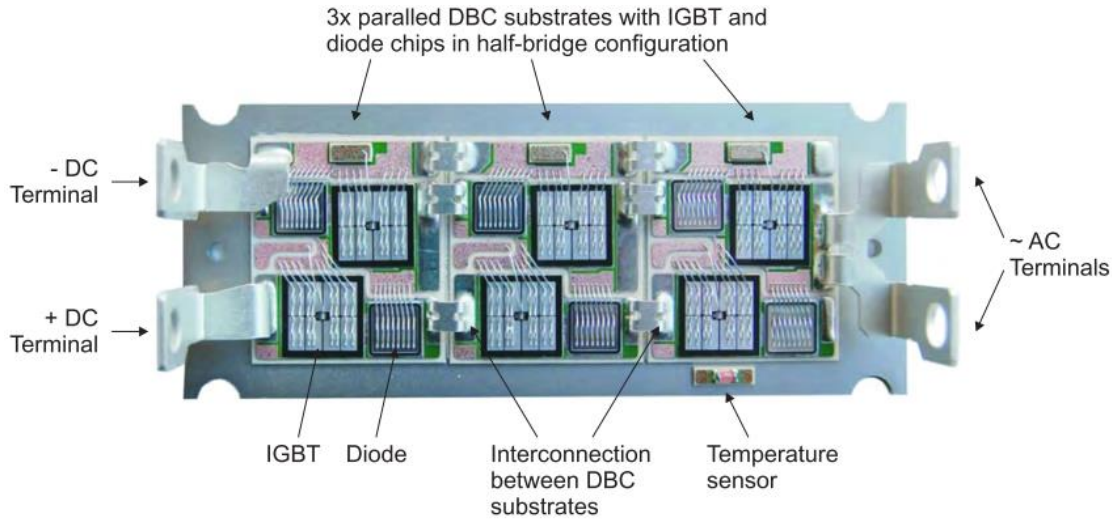


Figure 15. Opened IGBT module showing the packaged semiconductor chips, electrical terminals and a internal sensor for the base-plate temperature [39].

The devices packaged in this way are then encapsulated using either ceramic or plastic outer cover which is often filled with transparent silicone gel for complete protection of the die against environmental factors such as dust and humidity [23], [39].

The other more recently introduced type of packaging for IGBT devices is the press-pack [39], [76], [77]. It does not have soldered contacts which eliminates potential problems with mechanical fatigue and delamination. The press-pack also

boasts better thermal performance as it allows direct double-side cooling. Another feature of the press-pack is that the packaging does not provide electrical insulation and press-pack modules usually fail in short circuit mode (which can be a desirable feature in a number of converter designs incorporating redundancy).

Traditionally press-packaging has been used with other technologies such as diodes and thyristors – which are packaged as single-wafer devices. Large single-wafer IGBTs, however, are hard to manufacture and are not available, thus the typical IGBT press-packs, need to use multiple individual chips (they normally also include anti-parallel diodes chips – a requirement in most IGBT-based converter topologies). As mentioned earlier, the paralleling of multiple chips is necessary for achieving higher current carrying capability of the module. However, it also makes the adaptation of the press-pack capsules for IGBT devices a technological challenge which requires maintaining very tight tolerances for every aspect of the packaging [69]. On the one hand, the multiple chips and other parts need to be precisely aligned. On the other hand, the pressure applied to all individual chips needs to be maintained uniform to ensure they have identical electrical contact, as lower pressure on some of the chips will result in increase of their contact resistance and lead to unequal current sharing between the parallel devices.

Although there exist different innovative press-pack designs (such as the ABB StakPak, etc.), the basic concept of a press-pack is illustrated by Figure 16 below.

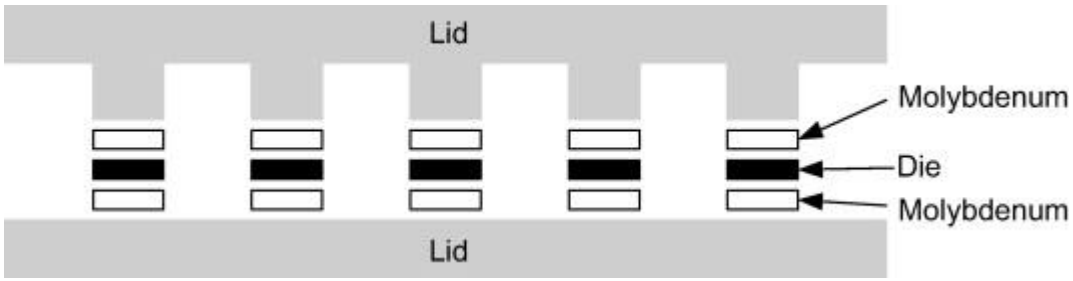


Figure 16. Press-pack – basic concept [78].

Its main components are the semiconductor chips themselves, the thin interface contacts (usually made of molybdenum) which sandwich and mechanically protect the chips, and the metal anode and cathode terminals (usually made of aluminium or copper) which are also the part of the press-pack encapsulation where the pressure is applied. Alignment frames or elements are used to position the chips relative to each other and their individual molybdenum contacts on the collector and emitter sides. Each of the emitter molybdenum squares has a small cut-out in one of their corners for the gate terminal. The gate connections are usually implemented with springs and guided by their own alignment frame. The metal terminals or lids compress the assembly together. Usually the collector side is one large flat plate, whereas the emitter side has raised pillars to allow some space for the gate connections. The lids provide both an electrical connection with the rest of the circuit and a pathway for the internally generated heat to exit.

The photos of open IGBT press-packs below (Figure 17) illustrate the actual internal structure of this type of packaging, the arrangement of the chips, the alignment elements, gate contacts, etc.

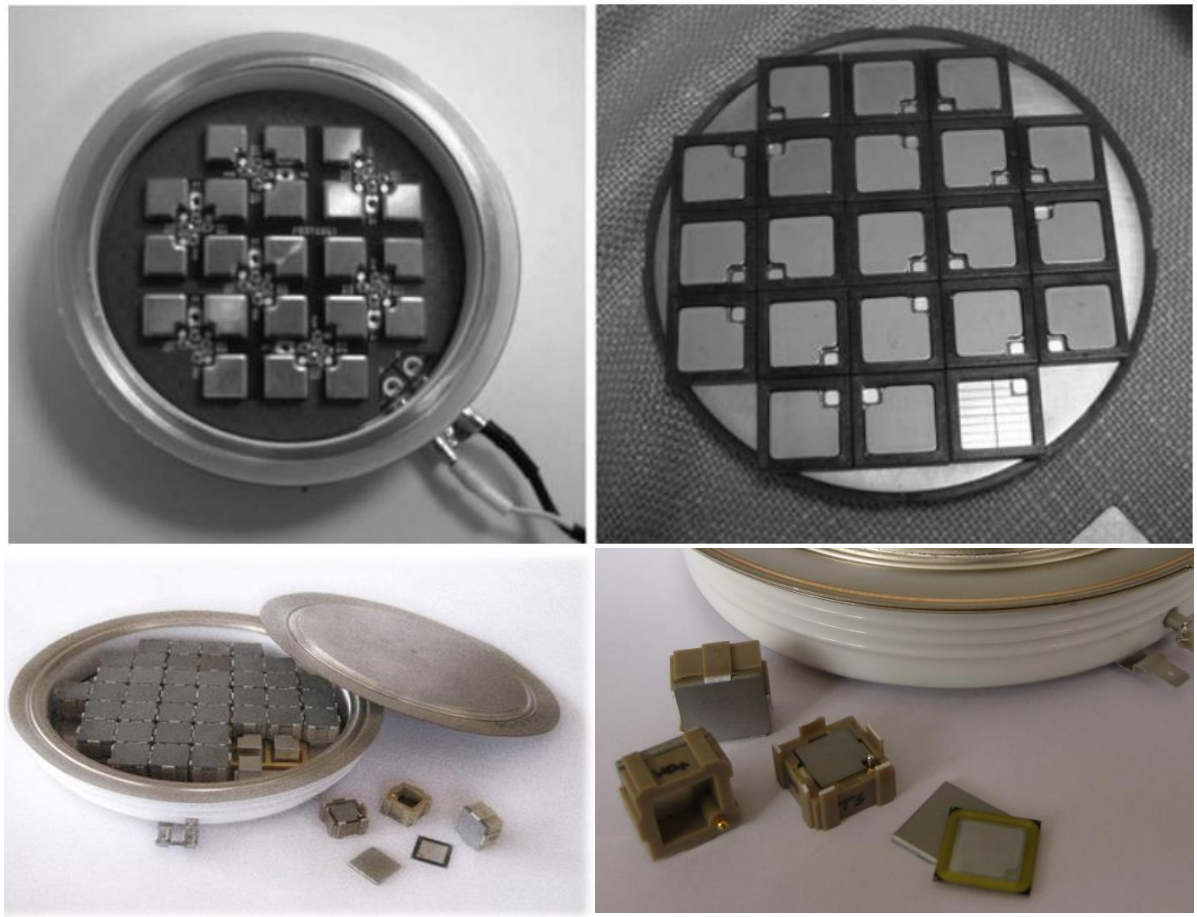


Figure 17. Open IGBT press-pack modules [69], [79].

For each of these two main types of packaging – DBC & bond-wire module and press-pack module – there exist a number of modifications to make them more reliable and/or increase their T_j limit for safe operation. For example DBC modules

sintering is used instead of solder to attach the die to its substrate, similarly printed bands can be used instead of wire bonds for the emitter contact, in press-pack modules there are optimisations such as individual pin springs for each chip, etc.

However, this project focuses on mainstream technology with the hope that, if a suitable practical solution for condition monitoring is found, it could also benefit other upgraded packaging versions. We will concentrate predominantly on the DBC & wire-bond module packaging and the reasons for this are as follows:

- This type of technology is still the most widely used in wind turbine converters to-date and our main industry contacts, Siemens Wind Power, use it in their converters.
- Manufacturers and technology experts claimed at a recent seminar on Power Electronics Packaging (organised by the ECPE (European Centre for Power Electronics) in Delft, Holland 2015) that "the future of the wire-bond module is the wire-bond module" – meaning that this type of technology will continue to be the most widely used technology because it still provides the best balance between functionality and cost-effectiveness.

2.3.3 IGBT device failure mechanisms

Since the focus of this project is condition monitoring a special point of interest here are the IGBT power devices failure mechanisms. Most studies

concerned with this topic such as [80] divide them into two main categories: chip related and packaging related failure mechanisms.

2.3.3.1 Chip-related failure mechanisms

The power device chip-related failure mechanisms include:

- Electrical Stress (In-Circuit) Failures such as damage caused by Electrical Overstress (EOS) and Electrostatic Discharge (ESD) and Latch-up resulting in dynamic avalanche;

- Gate Oxide Breakdown which can result from over-voltage stress that can result from EOS or ESD as described above or time-dependent dielectric breakdown (TDDB) that occurs gradually during operation;

- Other mechanisms associated with gate oxide degradation are the ionic contamination and charge injection including the mechanisms of slow trapping of electrons at the oxide interface, hot carrier injection and plasma damage.

- Failure mechanism resulting from defects of the crystalline lattice of the chip such as dislocations decorated with some metallic impurities. If they run across the device from collector to emitter, they can create current paths, known as pipes, allowing large leakage currents during the off-state and thus leading great power dissipation and device breakdown.

- Metallisation-related defects such as micro cracks affecting the current densities and electro-migration or the diffusion of the ions biased in the direction of the electron flow can also arise in the process of power (and thermal cycling) of the IGBT.

- Radiation can also cause device failure. Semiconductor devices are susceptible to two types of radiation:

  - external – (x-rays or cosmic rays from the operating environment);

  - intrinsic – from radioactive impurities (such as thorium and uranium) that may be present in the packaging materials. They can emit alpha-particles with energies up to 8MeV. Coating the chip with polyamides can provide some protection against them [81].

More information on those and other chip-related failure mechanisms can be found in [81], [82].

Overall it can be noted that the chip related mechanisms are complex, more than one can be active at the same time, for most of them the resulting failure modes are similar and therefore it can be hard to determine forensically which mechanism was at the root of the failure. Few of them are associated with gradual degradation; the majority of those failure mechanisms occur suddenly and therefore do not allowing tracking of changes for condition monitoring.

Harsh environmental conditions are also believed to trigger chip-related failure mechanisms [32] although it is yet unclear which ones; [80] reports a period of time with frequent lightning storms (known to create free ions) coinciding with higher rate of semiconductor failure and suggest that there might be a correlation.

There may still be unexplored ground for further research on the subject of chip-related failure mechanisms and more to add to our understanding of them. However, they are most often closely related to existing design or crystalline structure flaws and they tend to manifest suddenly, which defies the idea of condition monitoring. The current project does not aim to investigate device design and identify advantages or flaws. It aims to work with popular commercially available products and look for field-deployable on-line condition monitoring solutions for them, but such solutions can only deal with more gradual degradation processes. For these reasons here we will not focus further on the chip-related failure mechanisms of power modules.

2.3.3.2 Packaging related failure mechanisms

The failure mechanisms in this group are caused by the degradation of the power device packaging. Most of the up-to-date research on packaging related failure mechanisms focuses on the standard module packaging (with DBC substrate and wire bonds) which type has a complex sandwich-like structure containing a number of different material layers. Several major failure mechanisms have been identified for this type of packaging:

- Solder die-attach failure. It manifests as partial delamination resulting from the lateral growth and joining up of voids and cracks within the die-attach solder layer. The device is considered failed or damaged when its solder degradation is sufficient to cause a rise of 20% or above in its R_{th} (or V_{CE} respectively). More often, however, this type of degradation is not caught before it actually causes the chip to overheat and burn-out. The delamination can occur as a result of:

  - The thermo-mechanical stresses in the solder during the IGBT's operation (characterised by power and thermal cycling). These stresses arise from the different CTEs (coefficients of thermal expansion) of the solder and its adjoining materials. Their concentration is highest along the chip-solder interface where the most significant cracking and delamination takes place.

  - Effects of moisture ingress and expansion. It is possible for small amounts of atmospheric moisture to penetrate and get trapped in the packaging materials [37]. It can expands significantly during the thermal cycling of the device causing various failures including die-cracking (named "pop-corn effect" in [83], after the sound of the cracking).

  - Chemical corrosion enhanced by the temperature cycling, etc.

- Failure of the solder layer between the DBC and the base plate. The degradation/delamination mechanisms leading to the failure of the base-plate solder layer are the same as above, as well as the factors governing them. Here it is

important to note that because of the much larger surface area of this solder layer, the combined thermos-mechanical stresses it experiences are larger and can lead to faster delamination. This is why manufactures like Semikron are offering some power modules without a base-plate [39].

- Failure of the bond-wires. The bond-wires are responsible for providing the electrical connection to the emitter and gate terminals. Unlike the partial delamination of the die-attach solder, where sufficient electrical connection is still available to the collector terminal, the failure of one or more of the emitter bond-wires can lead to noticeable increase in the device's on-state voltage drop. The two ways in which the failure manifests are:

  - Lift-off – characterised by peeling and lifting of the wire's "heel" (where it joins to the metallisation finish on the IGBT chip emitter side).

  - Heel cracks – characterised by the grown of cracks in the heel of the wire that can lead to its lift-off or severing/breaking at the heel.

More detailed description of the packaging related failures are given in [20], [23], [24], [82], [84]. Degradation of elements external to the power module can also affect the converter safe operation and speed the power module's own degradation – examples include dust accumulation on air cooled heat sinks obstructing the heat exchange with the air, or the degradation of the thermal paste often used to provide a better interface between the metal surfaces of the heat sink and the

module's base plate (which on microscopic level are uneven and may not have good contact).

In general the packaging failure mechanisms refer either to the obstruction of either electrical current flow (as in the case of the bond wire lift-off) or the obstruction of the heat flow allowing the chip's cooling. In both cases the result is increased power losses and decreased efficiency. Therefore the power loss can be used as indicator for the device's health condition. What is significant about the packaging related failure mechanisms is that they occur as a result of material degradation or fatigue which is a process developing gradually over the lifetime of the device. Thus, they are highly suitable for condition monitoring.

In press-packs there are no soldered interfaces which allows the different elements to glide laterally with respect to each other during thermal expansion while maintaining contact [39], [76]. Because in press-packs solder fatigue and wire bond lift-off are no longer an issue, this type of packaging is considered more reliable. Also, the usual failure mode of the press-pack is short circuit which gives it an advantage for high voltage series connected applications over the conventional IGBT module, whose normal failure mode is open circuit. However, press-packs are not failure-proof; they just experience different failure mechanisms. Although it is more recent development in IGBT packaging and there is not much data regarding its failure rates and mechanisms yet [84], publications have already pointed out several concerns with press-packs reliability: [24] mentions that during the formation of the conducting alloy and at later operation

stages, molten aluminium attacking the molybdenum contact can form cracks in the plate, reducing its thermal conductivity and that the formation of intermetallics can also affect the electrical conductivity of the press-pack over time. Gate oxide damage and micro arcing have also been presented as two possible failure mechanisms in press-packs [78]. The last one is the result of thermally induced mechanical deformation of the clamping elements leading to partial loss pressure and therefore of contact between the chip and the molybdenum blocks and this has been mentioned as a common concern with press-pack by other publications as well [85], [86].

And like the conventional modules, press-packs can be subject to external reliability issues. As mentioned earlier the press-pack's outer case is electrically conductive and cannot be connected to traditional heat sinks. Large industrial press-pack converters are usually cooled by direct flow of non-conductive liquid, such as de-ionised water. Those systems need monitoring units that samples the cooling water and shuts down the converter, if the water dissolved particulates or the ion content reaches certain level when the water can potentially become conductive. Although this is not a failure as such, for offshore environments this can be a concern, since it is likely to necessitate human intervention (e.g. changing the liquid) [11].

Still, press-pack technology has its advantages and is likely to become a more and more common feature in future wind converters as the offshore wind turbines are getting larger and larger and moving from low to medium voltage drives. For

this reason, we will attempt to develop some further understanding of its packaging-related reliability issues (i.e. the partial loss of pressure contact and its implication for the paralleled semiconductor chips), although the main focus of this project will remain on the packing related failure mechanisms of standard DBC modules and the means for their health monitoring.

2.4 Thermal Behaviour and Modelling

Since the focus of this project is on thermally induced power module degradation and the development of temperature based condition monitoring that can tackle this problem in practical applications (i.e. offshore wind turbine frequency converters), the other type of background research highly relevant for this work are the publications on thermal behaviour and thermal management of semiconductors.

A lot about the theory behind semiconductor thermal behaviour and thermal modelling can be found in [87]. As mentioned earlier, semiconductor elements experience power losses when conducting electric current or switching. These losses are dissipated as heat which causes the junction temperature of the semiconductor to rise. Since the junction temperature is a parameter which influences both the semiconductor's electrical performance and the mechanical integrity of the packaged device, it must be kept below a specified safe operating limit by ensuring the heat is expelled from the working device at a sufficient rate.

To understand this process, it is necessary to refer to the underlying physical principles of heat transfer [88]. The main type of heat transfer observed in power modules is heat conduction. Heat conduction is internal energy transfer which arises due to a temperature gradient between two points in space and is achieved through microscopic diffusion and collisions of particles (molecules, atoms, electrons and phonons). It is predominantly observed within solid objects, or between objects that are in contact with each other (which represent the power module sandwich structure). Conduction can be described by Fourier's law stating that the local heat flux varies in proportion with the negative spatial temperature gradient:

$$q = -k\,\Delta T \qquad (1)$$

For simplified unidirectional heat conduction process this can be expressed as:

$$q = -k\left(\frac{dT}{dx}\right) \qquad (2)$$

Where:

q is the local heat flux density (the energy that flows per unit time through unit area) [W/m^2];

dT is the temperature spatial gradient [K/m];

d*x* is the distance in the direction of the heat flow;

k is the material's conductivity [W/mK]

The thermal conductivity k itself is a function of temperature. This is especially pronounced in solid insulators and crystalline materials like silicon:

$$k = k_{ref}\left(\frac{T}{T_{ref}}\right)^{\alpha} \quad (3)$$

Where:

k_{ref} = 154.86 for Si

α = 4/3 for Si

T_{ref} = 300K (The temperatures are in Kelvin)

The k value can also vary with orientation and spatial location in anisotropic and non-uniform materials. But it is often treated as a constant because its variation can be small over a given range of temperatures for some common materials. It must be established on a case per case basis whether k can be treated as a constant or not.

Heat conduction can also be described in terms of it being steady state or transient. In Steady State conduction the temperature may differ between any two points in space but at any one point in the system remains constant over time. Thus, the amount of heat entering any region of an object is equal to amount of heat coming out – i.e. there is equilibrium. During Transient conduction the

temperature of a point within the system will be changing with respect to time. This may occur when the temperatures of the initial and/or end nodes of the system change – which will cause a change in the rate of internal energy transfer. In this case the temperatures of all internal system nodes will change until a new equilibrium is achieved, (if the new amount of heat flowing through remains constant).

One of the most commonly used approaches for modelling heat conduction in semiconductor devices is by using equivalent thermal networks in which thermal phenomena are represented by analogous variables normally used to describe electrical circuits. Table 2 summarises the analogy between the two domains.

Table 2. Analogies between the electrical and thermal physical domains.

How is the variable measured w.r.t. a given node?	**Physical domain**	
	Electrical	Thermal
Through Variables	Current I (A)	Heat or Power dissipation P_d (W)
Across Variables	Voltage V (V)	Temperature T (K)

The property on the path from one node to another is dissipative in nature and describes the conductivity or storage capacity of the medium. In steady state conduction – equivalent to electrical DC conduction – the property of the material resisting the heat propagation is defined as thermal resistance R_{th} opposing the

heat flow (from the semiconductor power losses) between two points in space (for example the semiconductor P-N junction and the module's case directly under the chip) with temperature difference ΔT:

$$R_{th} = \frac{\Delta T}{P_{loss}} \qquad (4)$$

If P_{loss} [W] represents the heat flux q [W/m^2] from equation (2) divided by the area A [m^2] through which it passes (e.g. the collector side area of the semiconductor chip), the thermal resistance in one spatial dimension can also be represented as:

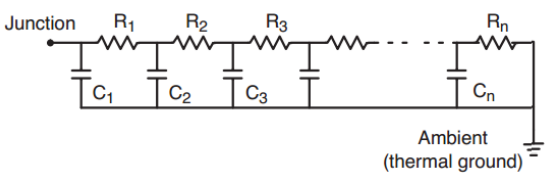
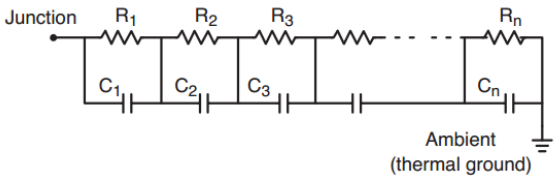
$$R_{th} = \frac{dx}{k\,A} \qquad (5)$$

The transient heat conduction is dominated by the heat storage property of the material – named thermal capacitance C_{th} in analogy with the electrical capacitance. It is in units of joule per Kelvin [J/K]. C_{th} is equal to the material's specific heat capacity (either mass or volumetric) multiplied by the amount of material involved in the heat transfer (either mass or volume). (In a similar manner one can derive a thermal parameter analogous to the electrical inductance [89], although such a parameter has not been found useful in describing practical thermal systems.)

Semiconductor thermal systems are traditionally modelled by two main types of RC equivalent circuits – both consisting of a number of stages with each stage including thermal resistance plus thermal capacitance. These two types are known

as Cauer and the Foster chain (or ladder) respectively. Cauer and Foster thermal models are also known as lumped element models, because of the symbolic division of the otherwise continuous in space physical system into a discrete number of resistive and capacitive elements wired together. Both networks can be used to model the same transient thermal response (or the thermal transfer function) of a system. The characteristics and differences between the two networks as well as the advantages and disadvantages of using either type are presented in the table below:

Table 3. Cauer and Foster chains comparison

• DESCRIPTION	
Cauer Ladder (grounded capacitor or continued fraction network):  	Foster Ladder (non-grounded capacitor or partial fraction network): 
Based on heat-transfer physics and reflects the physical set-up of the device: in multi-layer devices materials of different thermal capacities are connected through intermediary resistances. The R & C values can happen to coincide with resistance and capacitance of separate layers depending on the order of the network, but may also be in-between values or layer combinations.	**Schematic of the mathematical fit** to a real response transient curve (a plot of Z_{th} against time). A series of exponential terms consisting of amplitudes and time constants can be fitted to the curve and this can be represented as non-grounded capacitor RC network where amplitudes are R values and the time constant: $\tau = RC$

<table>
<tr><td colspan="2">• ADVANTAGES</td></tr>
<tr><td>• Can be used where the material characteristics of individual layer are known;

• Adequately estimates both end and internal node temperatures;

• It is easier to merge with another Cauer chain or use when parallel branches need to be connected to a common heat sink etc.</td><td>• R and C terms can be easily extracted from actual transient Z_{th} curves;

• Adequately estimates end node temperatures;

• The total equivalent impedance can be easily calculated by summing the individual RC level impedances: (6)

$$Z_{th}(t) = \sum_{i=1}^{n} R_{th\,i}(1 - e^{-t/R_{th}C_{th}})$$

• A lot of manufacturer's datasheets include Foster chain R & C values.</td></tr>
<tr><td colspan="2">• DISADVANTAGES</td></tr>
<tr><td>• The physical parameters for constructing a Cauer chain may not be easy to obtain and when available the correct mapping of thermal spread in individual layers is still problematic;

• The R and C parameter extraction from transient impedance is problematic and requires specialised software;

• Calculating the total transient thermal impedance is complicated and requires specialised circuit simulator;

• The time constant depends on

• It is difficult to transform into Foster (involving large errors)</td><td>• The internal R_{th}, C_{th} and node temperature values bear no physical reference to actual values and can appear in random sequence;

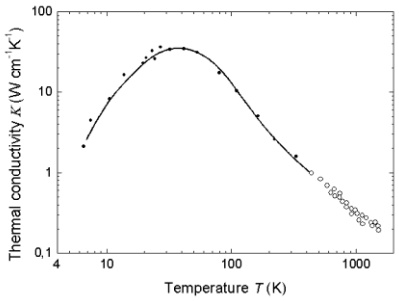
• It is more difficult to merge or model parallel Foster branches connected to common heat sink;

• Thus correct Foster models of IGBT & heatsink systems need to be derived from a curve of Z_{th} along the complete thermal path;

• It is difficult to transform into Cauer (involving large errors)</td></tr>
<tr><td colspan="2">• Both equivalent circuits suffer from the fact that a change of thermal resistance branch value affects the values in the other branches. A change of thermal resistance value outside the modelled part of the system has a similar effect.</td></tr>
</table>

Although electrical RC circuits are being used to model thermal systems, the analogy between the corresponding variables from the electrical and the thermal domains is not perfect. It is important to be aware of some important differences between the electrical and thermal resistance, as listed in Table 4 below.

Table 4. Specifics of thermal resistance as opposed to electrical resistance.

Thermal resistance	Electrical resistance
• Depends on the material's thermal conductivity which is temperature dependent as visible from the plot for Si below [90]. 	• Depends on the material's electrical conductivity, but is largely voltage independent (within the material's breakdown voltage limit).
• In a thermal RC circuit, <u>if resistances are added externally this</u> <u>will change existing R&C values in the model</u> (heatsink with smaller or larger heat transfer coefficient changes the model R_{th} values. The heatsink has a reverse effect on the thermal spreading within the IGBT and therefore on the time response and the resulting $R_{thj\text{-}c}$ of the IGBT. If the heat sink used later deviates from the heat sink used For example in the FEM model to extract R and C values for the thermal circuit, the model will not take this into consideration – i.e. the model with R & C as initially defined will be wrong. It must be pointed out that the <u>resistivity</u> of the material (apart from its temperature dependence) <u>has not changed</u>, but the <u>resistance</u> R_{th} changes as it is defined by	• In electrical network schematics single R values are not affected by adding extra resistors and capacitors to the network.

the equation (4): $$R_{th} = \Delta T_{j-a}/P_{loss}$$ and a different heat sink will absorb able to absorb and transfer out different amount of heat. While an air-cooled heat sink results in a wide spread of the heat flow in the module and therefore leads to calculating lower (i.e.better) $Rt_{hj\text{-}c}$, the limited heat spread in water-cooled heat sinks results in comparably higher $R_{thj\text{-}c}$ value from measurements. • Heat flow is 3Dimensional, but R_{th} is defined only in 2 dimensions (from point to point).R_{th} depends on the geometry of the system.	• The resistance does not depend on the 3D geometry of the electrical system.

The accuracy of any thermal model of IGBT power modules depends on the tracking the complete heat flow path from the junction to ambient in all directions, at the specific heat sinking arrangements and ambient conditions. Because good thermal models are heat sink and external conditions dependent any change in the complete thermal system for which the model was extracted will affect its accuracy. Thus, the Z_{th} curves presented in manufacturer's datasheets are fully correct and valid only for the cooling conditions at which they had been extracted (and which unfortunately the manufacturers do not specify as a rule). Therefore they must be used with caution and where possible the system designers should perform their

own tests on the complete system (including heat sink and casing) as it is going to be installed in the field.

In documentation published by ON-Semiconductors [91] it is demonstrated that the thermal impedance curves taken with different heat sinks coincide for an initial small period of time. After that they diverge and the difference is large. This shows that only until that point in time (up to which the curves coincide) the thermal impedance is due to the module packaging itself. This initial period of time is small – of the range of 0.2 seconds only (which time can be thought of as the module's time constant). After that the influence of the heat sink comes into effect. Still, it is important to note that the value of 0.2 s is orders of magnitude larger than the usual IGBT switching period and 10 times larger than the grid current waveform period (0.02 s). The period of lower frequency waveforms as might be present on the generator side are normally still lower than the power module's time constant (if the generator operates at only 12 Hz frequency, its sinusoidal current period will be 0.0833 s). This means that in most frequency converters the module's own heat storage capacitance will smooth out the instantaneous junction temperature peaks and troughs prevent it from experiencing internal temperature swings due to switching or the cyclic nature of the sinusoid current it conducts. In this case the thermal swings and cycles the module experiences will be the result of changing current levels (dependent on the change in wind conditions).

Only very low switching or sinusoidal current frequencies (of 5 Hz or less) will allow the module to start cooling before it starts conducting current and

heating itself again. Such conditions occur rarely, although they are possible – e.g. in VSC DFIG (Voltage Source Converter with Doubly-Fed Induction Generator) systems operating close to the synchronous speed the rotor side converter may experience very low AC side frequency while still conducting significant amount of current [11].

In general, for the purposes of condition monitoring working with instantaneous T_j measurements may not be practical – such measurements can only be obtained from open modules with thermal cameras. Contact thermal sensors such as thermocouples and thermistors have speed limitations (their thermal constant is rarely less than 0.5 s) [92], [93]. The estimation of average junction temperature $T_{j\text{-}ave}$ is something more reasonable to aspire to. Even if using TSEP which may be obtained at faster rate, we can still only estimate the $T_{j\text{-}ave}$ and not instantaneous values.

Working with very small internal thermal time constant for the IGBT module and much larger time constant for the periods in which parameters affecting the T_j – such as the current – change, we may be able to ignore the module's transient thermal response and consider only the steady state one – when only the R_{th} will influence the rate of heat flow. For example, when the wind turbine has been experiencing unchanging wind velocity for a few minutes or longer and its generator-side converter is operating at a frequency higher than 12 Hz, any T_j swings will be smoothed by the module's heat capacitance, which once saturated will stop affecting the heat flow, leaving the R_{th} as the only factor dictating how

fast the heat from the power losses can escape the module. This simplification is also commonly used by designers of thermal systems [91]. It may be of use for our work on thermal modelling and attempt at practical condition monitoring system.

More information on thermal modelling using lumped elements methods and RC systems can be found in [39], [69], [72] and various manufacturers application notes. This is the most widely used approach in industry as it provides simple and fast modelling of the thermal behaviour of semiconductors. The main limitations of this type of modelling is that RC networks is that they are not suitable for paralleling, and their accuracy is low for modelling three-dimensional thermal systems and systems with multiple heat sources. Still, they can produce very good results when modelling single devices.

More accurate thermal modelling can be performed with FEA (finite element analysis) software tools such as CADFEM, COMSOL or FloTherm. This type of modelling overcomes the limitations of the lumped element models, however its accuracy depends on the accuracy with which the internal structure and boundary conditions can be specified for the given thermal system and on the assumptions made about it [94], [95]. The FEA-based models run slowly and need a lot of processing power. In general they are confined to laboratory settings and deemed unsuitable for integration in practical on-line applications.

In conclusion, thermal modelling is an important topic for this project, because it provides a better understanding of the semiconductor device's operation,

junction temperature rise and what is necessary to keep it within safe limits. Although the thermal models discussed above may not fulfil the needs of a practical condition monitoring system, understanding them and making use of what is already known can help in discovering an alternative solution, as well as verifying its suitability for on-line condition monitoring in industrial application. Such thermal modelling solution will be computationally simple, yet able to handle multiple heat sources (as wind turbine converters often have multiple power modules cooled by a single heat sink).

Chapter

3 Electrothermal Modelling

The purpose of the modelling work presented here is to develop a better understanding of the electro-thermal behaviour of IGBT modules in practical converter applications. Also, as this project focuses upon systems of high power rating – i.e. wind turbine converters – in this case it was impossible to recreate them in lab conditions or observe their operation directly (either in the field, or in a testing facility setting). Thus, modelling was the only viable way to study them. Although this type of modelling may not represent entirely novel work or ideas, it is still a significant and necessary part of this project, as it was used to understand better the semiconductor power losses, what is meant by the converter operating point, which parameters describing this operating point will be subject to change in a real-life system and which – not, and which of them need to be incorporated in a practical condition monitoring scheme.

3.1 Modelling Converter Power Losses

Wind turbines can come with a number of different generator-converter arrangements [12], [67], [96]. Their power electronic converters can be fully rated (e.g. in systems with synchronous generators) or partially rated (e.g. in DFIG systems) and can have a number of different topologies, an overview of which including control capabilities and semiconductor subcomponents is given in [97]. The different topologies all have their advantages and disadvantages, but the focus of this project is not on converter designs, so we will not be discussing them here. We are interested in the performance of the semiconductor elements inside the converter and looking for condition monitoring solution that can hopefully target their degradation across various converter topologies.

As mentioned earlier, the medium-voltage drive designs using IGCTs have not yet gained popularity and wide deployment, the IGBT-based low-voltage drive designs continue to dominate the wind turbine converter industry. Therefore the focus of this work will be on IGBT converters. The topology selected here for the purposes of modelling is the 3-phase back-to-back 2-level bridge converter. Figure 18 below provides a schematic representation of this topology. The reasons behind this choice are that this topology is simple, well-understood, and one of the most popular topologies currently in use. Thus, modelling it will be sufficient for building up a good understanding of the actual operation of IGBT modules and the power losses they experience. Also, this is the topology used by our main industry contact –

Siemens Wind Power – in their own offshore wind turbines (in paralleled modular configurations to achieve the required power ratings) [98]. So in effect, using this design in our models will be representative of a realistic offshore wind converter scenario.

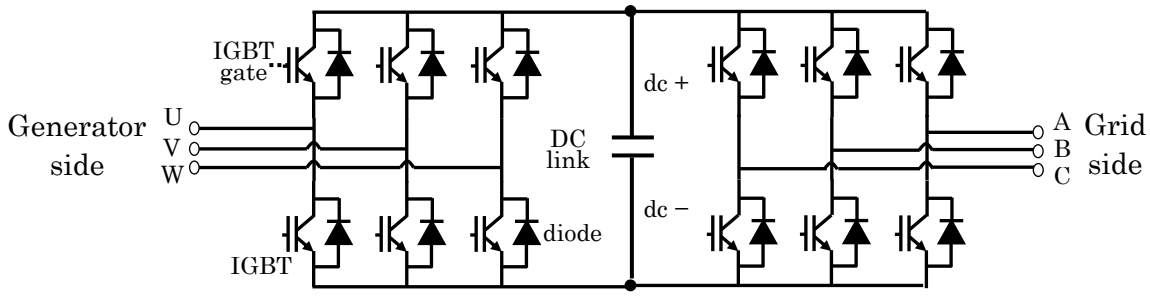


Figure 18. Two-level back-to-back 3-phase AC-DC-AC converter.

As the schematic in Figure 18 shows this converter type includes 6 bidirectional switches on the generator side (also known as rectifier stage) and 6 of the same type – on the grid side (also known as inverter stage), separated by a DC-link capacitor bank. In the case of the Siemens converters, as indeed in the majority of the larger industrial converters, each half-bridge leg is housed in a separate power module, although there exist power modules housing a complete rectifier or inverter stage, or the whole AC-DC-AC configuration. Our models were based on modules of different type, number of switches per module and rating, but still followed this 2-level 3-phase topology

The modelling software used was MATLAB with Simulink. Since the main focus of the modelling work was not on converter design and control, but the aim was simply to observe the electrical signals through the semiconductor devices and their respective power losses, the modelling was broken down in stages. The very first model included only the inverter stage – as shown in the screenshot image in Figure 19.

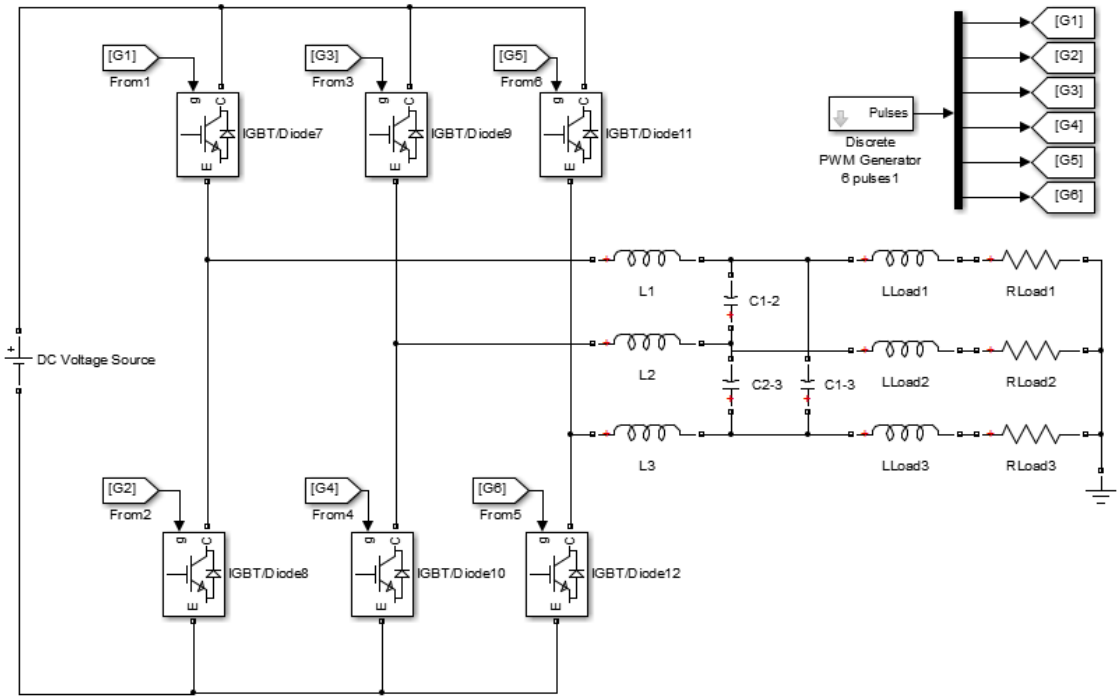


Figure 19. Screenshot of Simulink model representing the inverter stage only.

The model is based on ideal switches, so in order to estimate the power losses of the IGBT and diode devices, Look-Up Tables (LUTs) are extracted from the module's datasheet graphs. For the IGBT the graphs used are as follows:

- The on-state collector-emitter voltage V_{CE} versus the collector current I_C at different T_j.
- The I_C versus the switching energy losses – E_{ON} and E_{OFF} at different T_j.

For the diode the graphs used are as follows:

- The forward diode voltage V_F versus the diode current I_F at different T_j
- The I_D versus the diode's reverse recovery energy loss E_{rr} at different T_j.

The reverse recovery power loss of the diode occurs when the diode switches from conducting to blocking mode. The loss in the diode which occurs when it begins to conduct, unlike the IGBT E_{ON} loss, is considered negligible and manufacturers do not normally publish any data about it. Thus, as a rule, it is ignored in similar types of power loss modelling.

In our models, the conduction power losses were obtained using following algorithm (applied in the Simulink model as presented by Figure 20 below):

1. Check whether the device is conducting or not (see Table 5 below).
2. Input the instantaneous current value in the LUT to obtain on-state voltage. (In the very first models a set value was used for the T_j, later on thermal model and T_j feed-back loop were added, enabling the use of 2D LUTs with T_j being the second input to the table.)
3. When the device is conducting only, multiply the current and the voltage.

4. Apply this process simultaneously for each of the 12 semiconductor devices (6 IGBTs and 6 diodes) in the simulation.

5. Add the resulting waveforms to get the total conduction loss.

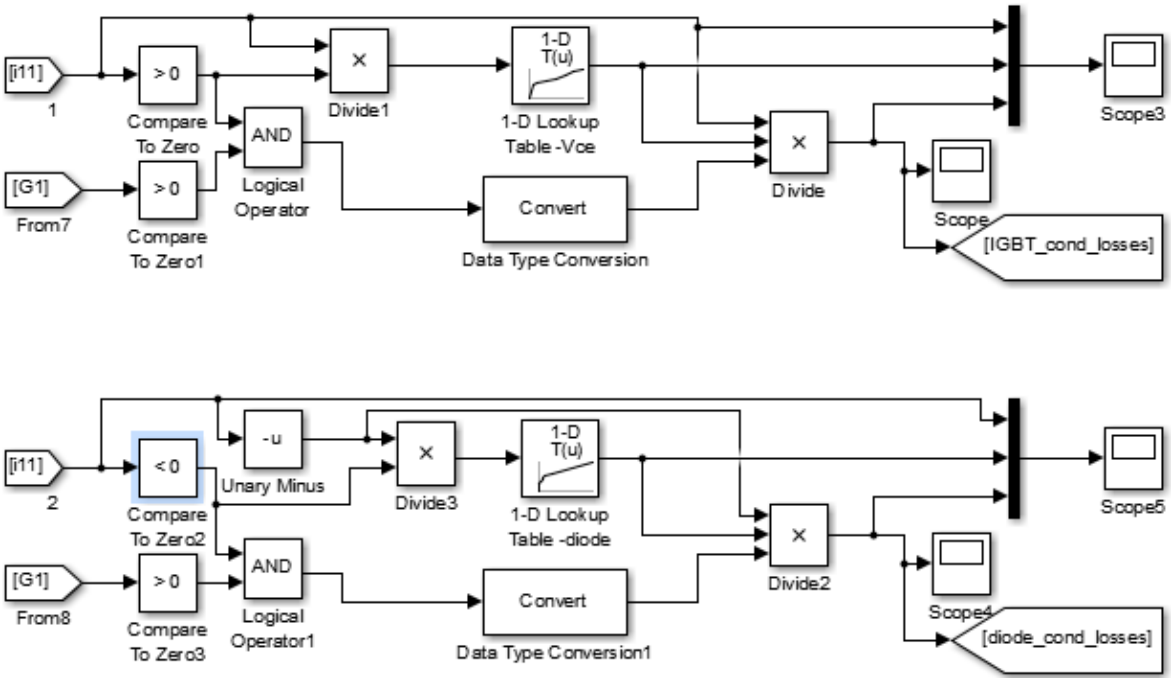


Figure 20. Part of the Simulink model block diagram illustrating the logic of the conduction losses calculation for one IGBT & free-wheeling diode pair.

Table 5. Conduction within one phase leg of the 3-phase 2-level inverter determined by the gate state and the load current sign.

Gate 1	Gate 2	Current	IGBT 1	Diode 1	IGBT 2	Diode 2
ON	OFF	positive half cycle	Conducting	Blocking	Blocking	Blocking
ON	OFF	negative half cycle	Blocking	Conducting	Blocking	Blocking
OFF	ON	positive half cycle	Blocking	Blocking	Blocking	Conducting
OFF	ON	negative half cycle	Blocking	Blocking	Conducting	Blocking

The first power module modelled was a complete 3-phase inverter packaged in one relatively small module SK35GD126ET, which was used by COMPERE to demonstrate their proposed temperature-based condition monitoring method. The power loss obtained from the modelling of its conduction loss is given in Figure 21 below. It is a waveform with a value of zero when the device is OFF (or blocking the current flowing in the reverse direction) which otherwise follows the general sinusoidal shape of the load current, interrupted by the switching events. The figure also shows for comparison the current curve and the small V_{CE} value extracted from the LUT.

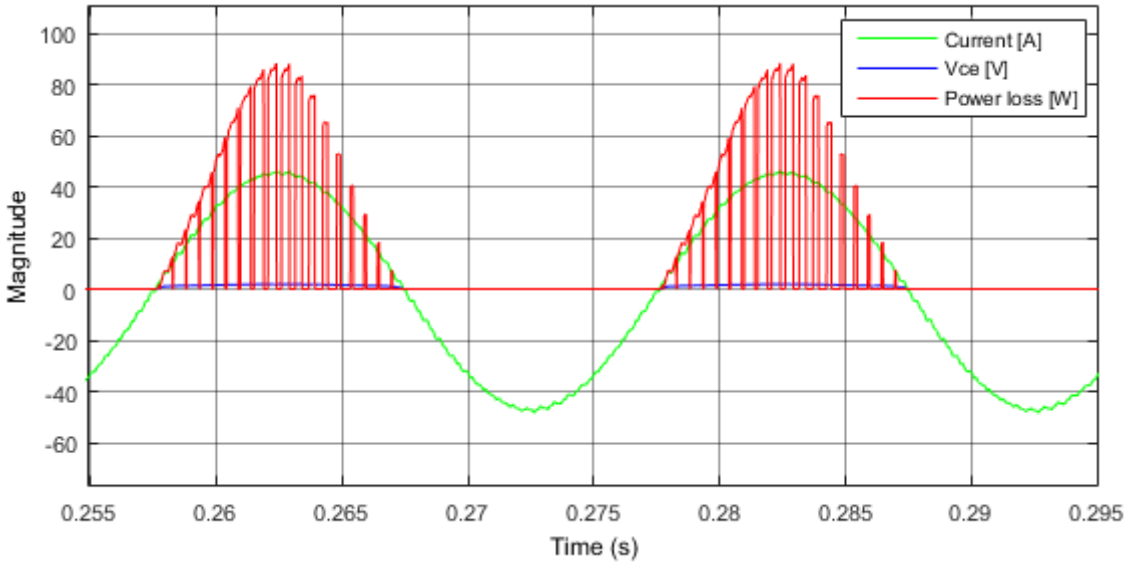


Figure 21. Conduction power loss from Simulink model of the top IGBT in the first half-bridge leg – conducting in the positive half cycle of the RMS current.

It is worth noting that when the top IGBT conducts and experiences power losses, it is the antiparallel diode adjacent to the bottom IGBT of the half-bridge leg

which also conducts and experiences power losses when the top IGBT is switched off (as shown in Figure 22 below). That is, the IGBT and its adjacent anti-parallel diode conduct during different half cycles of the sinusoidal current. Thus, the top diode passes current and dissipates power during the negative current half-cycle (as shown in Figure 23 below). If the top IGBT and top diode chip of the half-bridge leg are positioned physically close together, this may mean that they are experiencing more uniform temperature due to the heating effect of their neighbouring device while they themselves are not conducting.

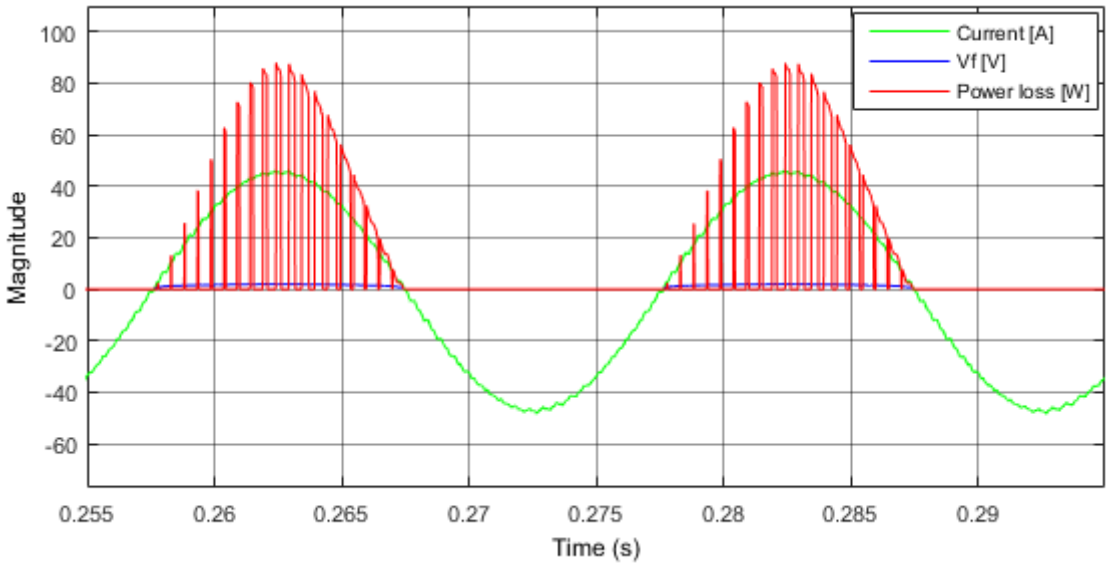


Figure 22. Conduction power loss from Simulink model of the bottom diode in the first half-bridge leg – conducting also in the positive half cycle of the RMS current.

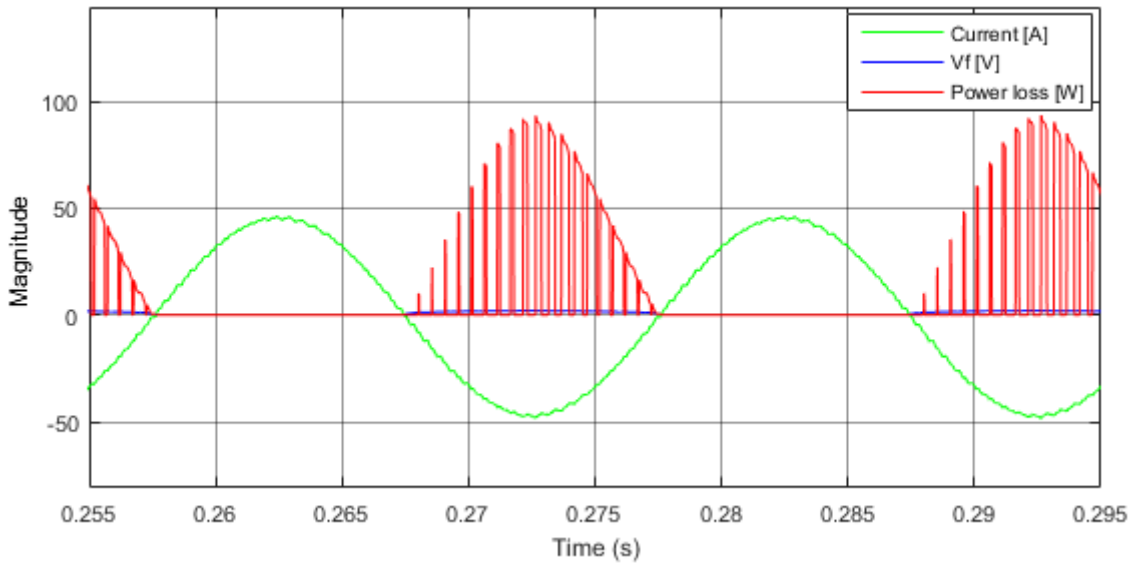


Figure 23. Conduction loss from Simulink model of the top diode in the first half-bridge leg – conducting in the negative half cycle of the RMS current.

Another thing which becomes obvious from the conduction power loss waveform even in this simple model is the fact that the portion of the switching period during which the top IGBT is ON and conducting is changing – it can be seen that its duty ratio becomes smaller as the positive current decreases towards zero while at the same time, the duty ratio of the bottom diode (also conducting in the positive half cycle of the RMS current) increases. This was found to occur when there is a phase shift between the waveforms of the current and the fundamental voltage – as seen from the IGBT. The shift in the model is introduced by the presence of the inductive and capacitive passive filter components. This effect related to the power factor cos φ needs to be further investigated, as it determines whether the IGBT or its non-adjacent diode is conducting and therefore heating more.

Apart from the conduction losses there are also switching losses experienced by the IGBT and diode devices. In reality the switching power loss comes as two short spikes (lasting in the range of nano- or micro-seconds) at the beginning and the end of the conduction period for the IGBT and mostly localised at the end of the conduction period of the diode (the reverse recovery loss). The practical approach adopted for their modelling here, however, does not attempt to replicate their spike shape as this would mean using very small time steps and over complication of the model in general. Instead they are estimated as an average power loss value over the whole switching period. This may indeed men that the model does not account for the instantaneous high current and voltage spikes experienced by the semiconductors at the start and end of conduction, but in terms of thermal effects (which as mentioned earlier have much longer time constant than electrical ones) this averaging over the switching period is justified.

The extraction of the switching losses in the model (illustrated by Figure 24 below) is again based on using LUTs extracted from datasheet graphs with the phase current as the input parameter (as mentioned earlier, initially a set value was used for the T_j and subsequently it was added as the second input to 2D LUTs). The algorithm includes the following steps:

1. Check whether the device is active/conducting during the current half cycle (positive or negative) of the RMS current.

2. If no, no switching losses are calculated and added, if yes, use the device's gate turn-on or turn-off event as a trigger calculate and add switching losses (for the diode we use the gate signal of its adjacent IGBT as trigger).

3. Input the instantaneous RMS current value into the switching loss LUTs. For convenience the LUT results can be summed together at this stage.

4. As the datasheet usually publish current versus switching energy in units of J or mJ, we need to find the corresponding power. This is done by multiplying the LUT switching energy result by the switching frequency which gives the energy dissipation rate in units of J/s or W.

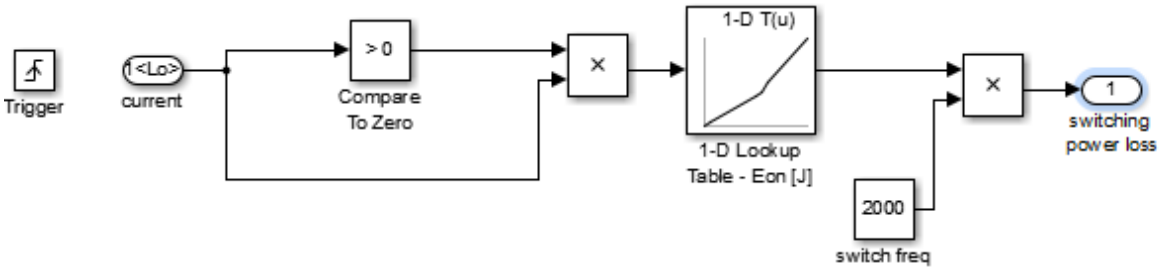


Figure 24. Simulink model portion of the block diagram illustrating the extraction of switching losses.

The resultant wave form has a step-like appearance (due to the averaging over a switching period), but again follows the rise and fall of the current. Aside from the current, the switching losses depend on the DC link voltage V_{DC}, the switching frequency f_{sw} and the T_j [39]. As the first V_{DC} is usually tightly controlled and the f_{sw} is normally fixed, the fluctuations of the current and T_j remain the factors governing the fluctuations in the switching losses. To recall, the variable operating point

parameters governing the conduction losses are again the current and the Tj, as well as the cos φ which does not have direct effect on the switching losses. (The IGBT's on-state gate voltage V_{GE} is another parameter which affects I_C-V_{CE} relationship and thus the IGBT's on-state power losses, but since unlike the current, temperature and power factor, it has a set value by converter design, we will not be modelling effects of its variation.)

Following the basic principles above, other more elaborate electrical models were also developed for different modules (including the power modules used in the Siemens converters), for the rectifier stage operating at lower RMS current frequencies, etc., but the further electrical loss modelling was undertaken mainly with the goal to understand better the influence of the power factor cos φ or the phase shift between current and voltage.

3.2 Influence of the Phase Shift between Voltage and Current (cos φ) on the Conduction Loss

A mention of the cos φ influence on the conducting behaviour of IGBTs and diodes can be found in [39], [99], confirming that it arises from a phase shift between the sinusoidal current waveform and the fundamental sinusoidal component of the PWM square wave voltage across the devices in a phase leg – as illustrated by Figure 25:

• When the waveforms of the current i_L and resultant sinusoidal voltage V_{out} are both positive, it is the top IGBT in the phase leg that predominantly conducts the current.

• When the i_L is positive, but the V_{out} has gone into the negative quadrant the bottom diode predominantly conducts.

• When both waveforms are negative, the bottom IGBT predominantly conducts.

• When i_L is negative, but the voltage is positive, the top diode predominantly conducts.

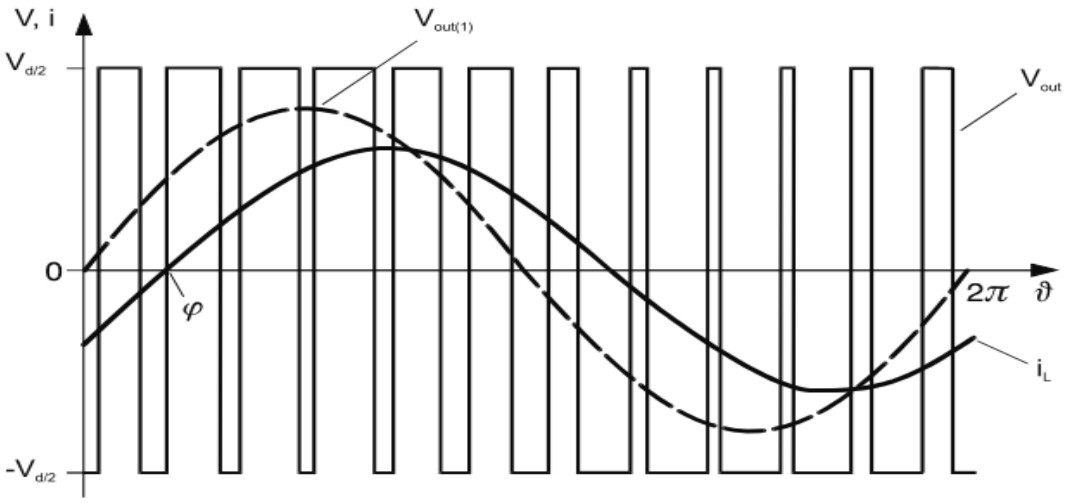


Figure 25. Basic circuit of a converter phase with 2 IGBTs and 2 freewheeling diodes [99].

To explore this relationship between the phase shift between the current and the voltage and the conduction power losses another electrical model of the 2-level 3-

phase system was developed in Simulink allowing selective changing of cos φ – which here refers to the phase shift between voltage and current as seen by the semiconductor elements. The results (as illustrated by Figure 26 below) show that indeed the closest to 1 the cos φ is (i.e. during operation in inverter mode) – the more losses are experienced by the IGBT and vice versa – the closest to −1 the cos φ is (i.e. during operation in rectifier mode) – the more losses occur within the diode. Also, the phase shift results in a shift of the timing of the losses.

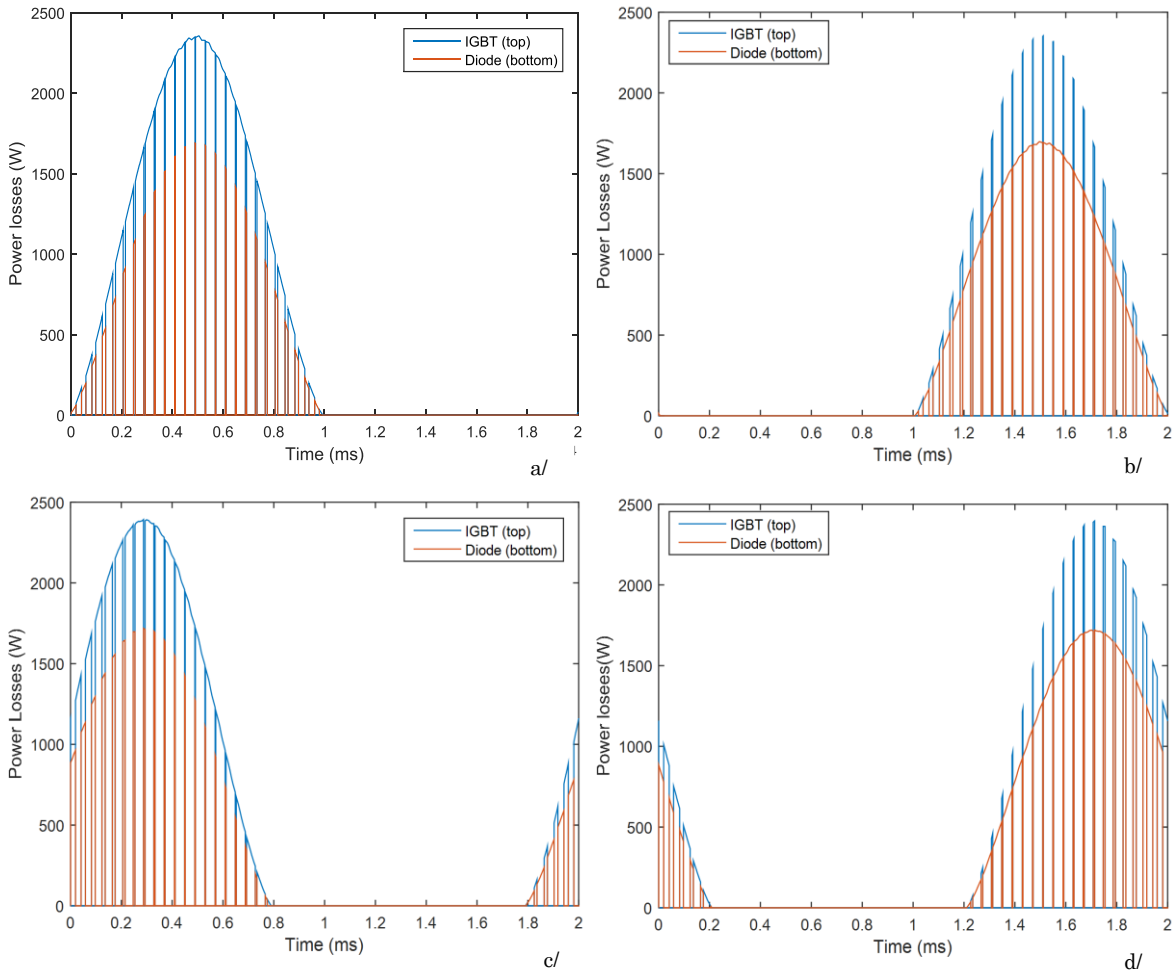


Figure 26. Power loss plots from Simulink model exploring the effect of cos φ: a/cos φ = 1 (maximum IGBT losses); b/cos φ =−1 (maximum diode losses); c/cos φ = 0.85 (high IGBT losses); d/cos φ =−0.85 (high diode losses)
Model – based on Infineon H-B module FF1000R17IE4D_B2 (1000A, 1200V_{dc})

During the development of this model, it became clear that the phase shift denoted above as cos φ should not be mixed with the grid, load or generator power factor. They will also affect cos φ within the semiconductor elements, but, they do not coincide with it. For example, when the load power factor equals 1, the IGBT in

an inverter will still be experiencing some phase shift between the current and the voltage across is due to the influence of the inductive and capacitive elements in the converter filter. Our model does not include external power factors, as cos φ is simply used to represent total effect that any external phase shift scenarios can have on the semiconductors.

Figure 27 below illustrates how the IGBT and diode power losses change with their changing cos φ. It is based on another module – Infineon FP75R12KE3 (rated at 75A, 1200V_{dc}).

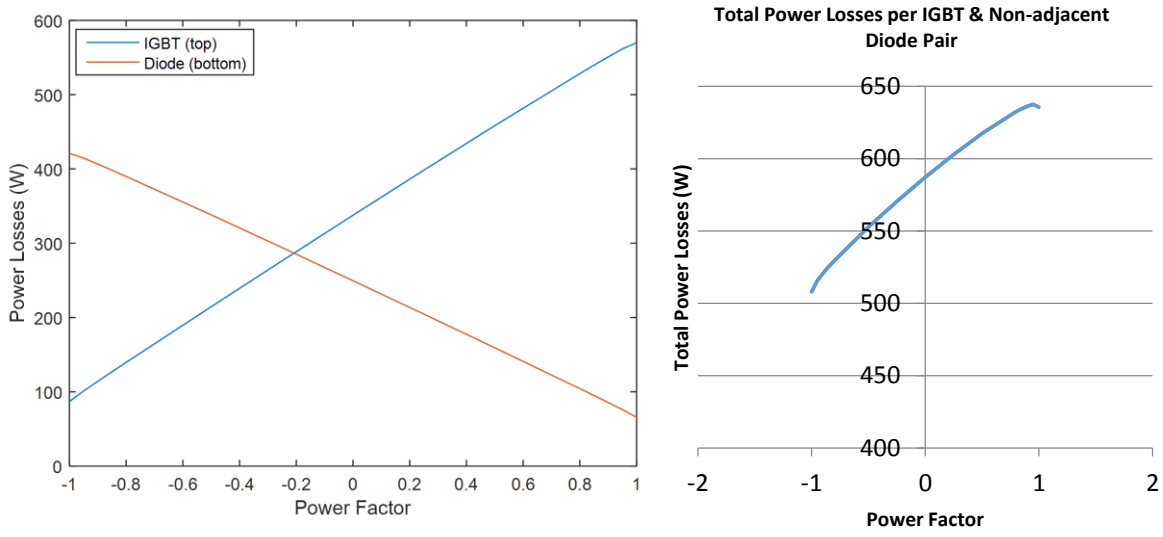


Figure 27. Influence of the phase shift between current and fundamental voltage component as seen by the IGBT/diode on their conduction losses.

As the diode conduction losses are lower, the module will experience its lowest total power losses when operating in rectifier mode (close to cos φ = −1). What is interesting is that in inverter mode, operating at lower internal cos φ (which may be

due to lower external power factor – something undesirable in the grid) can actually be beneficial for the module, as it can reduce its overall power losses and therefore its operating T_j.

The modelling results also demonstrate that there is an additional factor affecting the conduction losses. This is the modulation index in PWM converters which determines the device duty cycle duration. For example, a modulation index 0.8 means that when the current and voltage are in phase, at peak positive current, the top IGBT will be conducting only 90% of the switching period. For the remaining 10% of the time it is OFF and the current is diverted via the bottom diode. (This is why above it was specified that when both current and voltage waveforms are in the positive quadrant the top IGBT conducts "predominantly".) For a modulation index 0.9, the IGBT OFF-cycle is reduced to 5% of the switching period. Thus, the closer to 1 the modulation index, the higher the power losses will be if the converter operates in inverter mode (IGBTs conducting larger portion of the current), but at the same time the lower those losses will be if the converter operates in rectifier mode (diodes conducting most of the current). This is due to the fact that for the same current level the IGBT conduction losses exceed those of the diode (at least for the physical devices modelled so far).

This finding is confirmed by [39] which suggests using the product of the modulation index (m) and cos φ :

- $m \cdot \cos \varphi = 1$ results in maximum on-state losses
- $m \cdot \cos \varphi = -1$ results in minimum on-state losses

The above relationships can be of use, if the modulation index adopted by the converter control scheme is subject to variation. If it is a fixed value then the power factor cos φ remains the only other variable, aside from the current and T_j influencing the semiconductor on-state loss and as such it needs to considered in potential condition monitoring systems.

3.3 Simplified Mathematical Model

Having established the factors that govern the fluctuation of the electrical losses experienced by an IGBT module operating inside a converter, it is possible to simplify its power loss modelling by removing the simulated electrical system altogether. It can be substituted by mathematical and logical expressions producing the signals necessary for the power loss estimation.

Such Simulink model was developed based on datasheet extracted LUTs for the Infineon half-bridge module FF1000R17IE4D_B2 (used on the rectifier side in the Siemens offshore wind turbine converters). For this model, all the necessary starting parameters needed to mathematically recreate the sinusoidal current signal are the RMS current value, the fundamental frequency – 50 Hz, the switching frequency and the modulation index. This signal is then fed into the LUTs to obtain the conduction and switching losses of the module. With an added thermal model and feed-back loop, the T_j can also be estimated in parallel and supplied as the second input of the 2D LUTs. (The next section will focus on the thermal modelling.)

The thus simplified Simulink model has a dramatically improved run time. The system errors arising from the modelling of the electrical components in the earlier model versions have also been eliminated by the simplification of the model. The much reduced simulation time allows many input parameter variations to be swiftly explored. For example, for peak current of 1000A, switching frequency 2500 Hz, modulation index 0.8, fundamental frequency 12 Hz, power factor 1 and water cooled heat sink with maximum temperature of the inlet water maintained below 75 deg C°, we can quickly get an estimate of the IGBT-diode pair power loss (Figure 28) and junction temperature (Figure 29) (assuming close proximity of IGBT and diode chips and module capacitance temperature smoothing effects). This type of model proves valuable for quick experimentation with a range of values to demonstrate their effect upon the heating losses and internal module temperature.

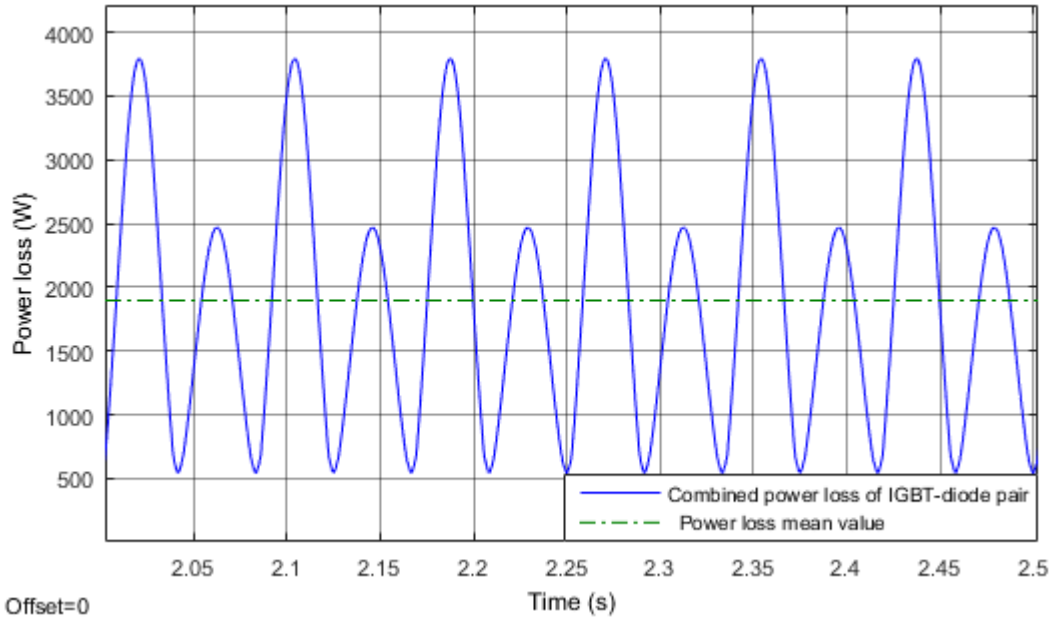


Figure 28. Total power loss curve example obtained from simplified maths model.

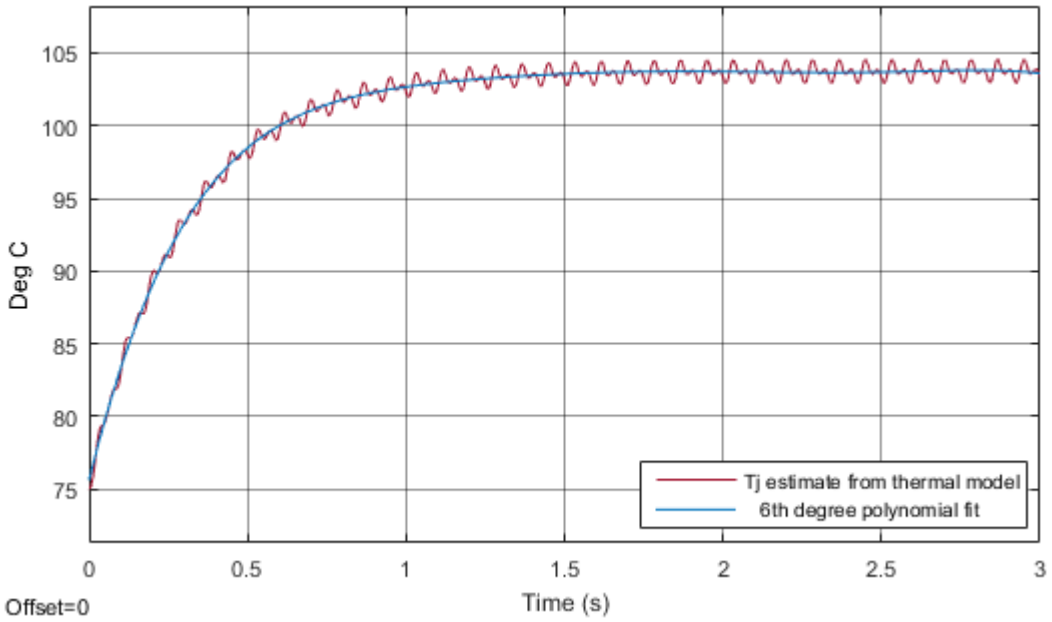


Figure 29. IGBT Tj curve example obtained from simplified math model

3.4 Thermal Modelling with Feedback

The junction temperature of the semiconductor T_j is an important parameter influencing its electrical power losses to such an extent that its electrical and thermal behaviour realistically cannot be decoupled. In simple models one can assume steady state operation of a device and obtain the its electrical power losses using only the sinusoidal phase current as a variable LUT input, but the result's dependency on the T_j is still implied since it is valid only for a given average T_j value (e.g. our earliest converter power loss models assumed device operation at a T_j of 125 °C). However, this approach will not be valid any more, if the model intends to:

- use changing RMS current levels or any other changing electrical parameter which can affect the power losses (changing the average power loss level will mean changes in the average internal heat dissipation and therefore changes in the average T_j as well, so the assumption that the device is operating at a set average T_j level will not be valid any more);
- or specifically demonstrate the change of T_j (e.g. from cold start, etc.) and explore the relationship between the T_j and the power losses.

In those cases it will be necessary use the output of the electrical model as input into a thermal model to estimate T_j from the power losses. The T_j will be then fed back in successive model iterations as LUT input into the algorithm for

estimation of the power losses. Such thermal models were integrated into the later power loss models developed during this project. The thermal model used are in the form of the traditional lumped-element networks which can be easily implemented in Simulink using electrical resistors and capacitors to represent thermal resistances and thermal capacitances, a controlled current source to represent the power losses (or heat) generated inside the semiconductor, and a DC voltage source to represent the ambient temperature outside the thermal system of interest.

Both Foster and Cauer networks have been tested in the process of modelling. Foster networks were extracted based on the datasheet thermal impedance Z_{th} curves and tables where available. For example, the FF1000R17IE4D_B2 datasheet also provided R_{th} and τ values for a four-stage Foster network from junction to module case. The disadvantage of using such a Foster network, however, is that it does not model the complete heat flow path and its output is therefore unrealistic. Moreover, it cannot be expanded by adding extra RC stages or by adding on to it a Cauer network of the heat sink. As the Foster network is a mathematical curve fit and its segments have no correlation to physical structure, adding new segments will only render the fit invalid. Foster networks are useful only when they model a complete heat flow path. On the one hand, it is understandable why manufacturers do not provide junction-to-ambient impedance curves and Foster parameters – after all their modules can be used with different heat sinks and the published impedance curves will not be representative. But on the other hand, Foster thermal models

from junction to case are only really useful for exploratory exercises in thermal modelling.

Cauer thermal networks were also explored in the electro-thermal modelling stage of this project. Unlike the Foster ladders, they are physics based and their RC segments bear correspondence to the device's internal structure. Figure 30 presents an example of one such Cauer network extracted for an IGBT chip inside a DBC-type module on a water-cooled heat sink. As can be seen from Figure 30, each material layer is represented by one R_{th}-C_{th} rung of the ladder (although splitting thicker layers into several R_{th}-C_{th} segments sometimes is also done in Cauer models) and the result is a 9^{th} order model.

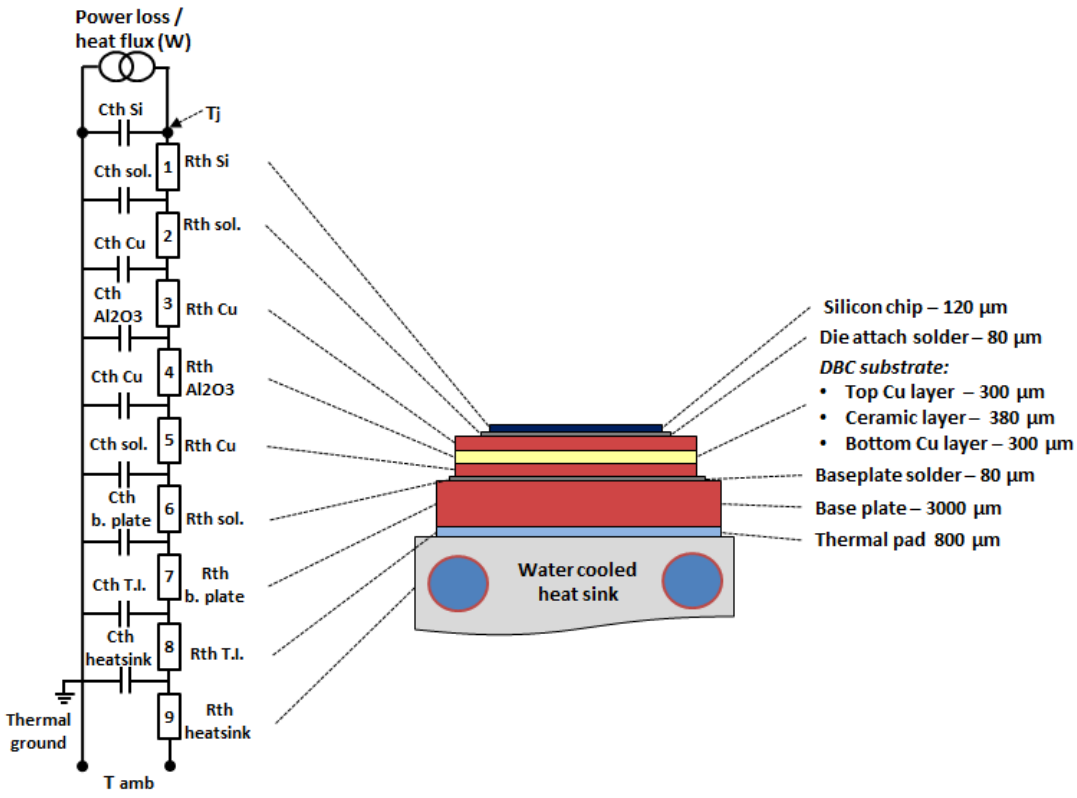


Figure 30. Cauer network based on material properties and physical dimensions

The module used for this model is the Semikron SKM50GB12T4 (50A, 1200V) – as shown in Figure 31 below with its exposed internal DBC layout and a highlighted IGBT chip. The module was opened to study its internal structure and chip dimensions which were then used to calculate the R_{th} and C_{th} values for the Cauer ladder.

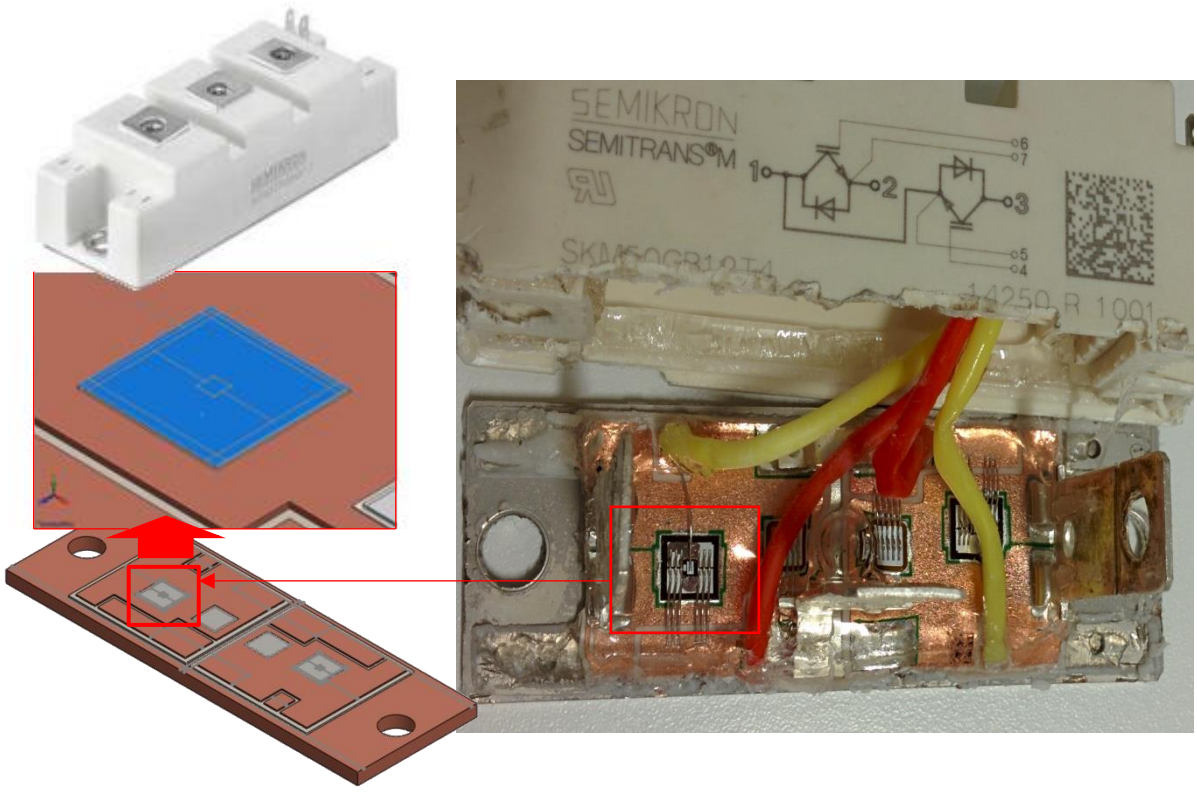


Figure 31. SKM50GB12T4 module – internal layout module highlighting the IGBT chip modelled using Cauer network.

Those values are derived following a process described in [39]. The thermal capacitances are calculated from the material's volumetric specific heat capacity (s) and the volume of each corresponding layer (V):

$$C_{th} = sV \qquad (7)$$

The thermal resistances are calculated across the two adjacent layers – from the centre of one to the centre of the other. This is because we are interested in obtaining the temperature of the layer itself – not the interface between two layers – and the most representative physical position of such temperature measurement will be midway through the layer. The R_{th} is thus the combined thermal resistance of the bottom half of the first layer and top half of the following layer – calculated again using layer dimensions (thickness and area) and the material heat resistivity value (k) :

$$R_{th} = \frac{d_1}{2k_1A_1} + \frac{d_2}{2k_2A_2} \qquad (8)$$

The figure below illustrates the idea behind the R_{th} and C_{th} extraction.

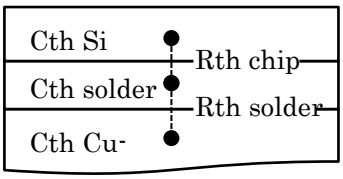


Figure 32. C_{th} is calculated as internal to each layer and R_{th} is calculated across two adjacent layers. T_j will be the first point corresponding to the node between the first C_{th} and R_{th} branch.

Table 6 below contains the extracted R_{th} and C_{th} values for the IGBT Cauer model.

Table 6. Cauer network R_{th} and C_{th} parameter extraction.

Layer #	Material	Area (measured) A [m^2]	Thickness (measured) d [m]	Heat conductivity from [39] k [W/(m·K)]	Heat capacity from [39] s [Ws/(K·m^3)]	Thermal resistance (calculated) R_{th} = d/(k·A) [K/W]	Thermal capacitance (calculated) C_{th} = s·A·d [W·s/K]
1	Si chip	5E-05	1E-04	125	1650000	0.02018	0.01005
2	Solder	5E-05	8E-05	70	1670000	0.01123	0.00712
3	Cu1	0.0007	3E-04	397	3421000	0.00978	0.76049
4	Al2O3	0.0009	4E-04	24	3025000	0.00978	0.98167
5	Cu2	0.0007	3E-04	397	3421000	0.00123	0.76049
6	Solder	0.0008	8E-05	70	1670000	0.00206	0.10641
7	Cu base plate	0.0028	0.003	397	3421000	0.02133	28.95192
8	Thermal Pad	0.0028	2E-04	1.8	1200000	0.02096	0.68720
9	Al heat sink	0.0387	0.016	212	2480000	0.00097	1527.39852
JUNCTION TO HEAT SINK TOTAL R_{th}						0.09752	

Thermal modelling with Cauer networks is based on the assumptions that the heat flux propagation is one-dimensional and unidirectional – i.e. from the chip junction through the module base plate and into the heat sink – and that there is no significant thermal interference between different semiconductor chips. Although these assumption may appear as an over simplification of the thermal system, they

may be deemed reasonable, as laboratory experiments using the exact type of power module and heat sink for which the thermal model was derived have shown that the water-cooling system draws the heat out efficiently with relatively small thermal time constant which minimises the lateral heat spread and temperature build-up that can be observed in air-cooled heat sinks.

It was found that higher order Cauer models can be simplified (as shown in Figure 33) by adding all thermal resistances together in one lump sum and finding a single thermal capacitance value which together with the lumped thermal resistance produces a close enough match to the response of the higher order model describing the rise of junction temperature with time.

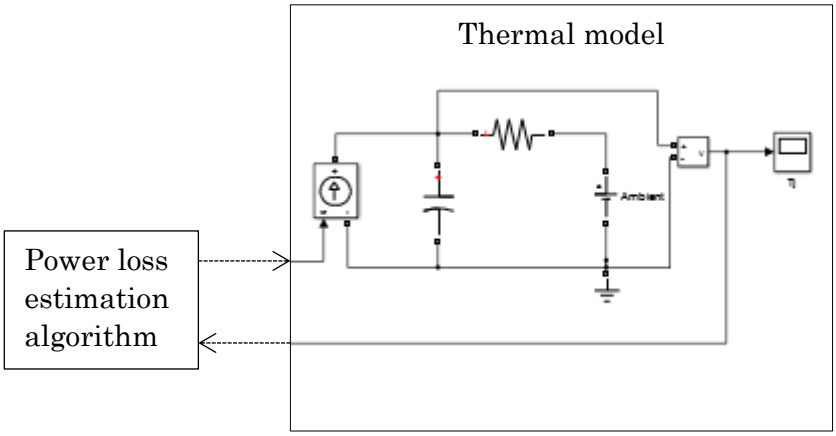


Figure 33. Simplified first order thermal model that can be used to replace higher order Cauer networks in steady-state electrothermal models.

It is true that the exact shape of the curve of the higher order model response will be slightly different to that of the first order model, but if we are only interested

in the steady state T_j and both responses arrive at this steady state value at almost the same time, the inaccuracy of the simplified model will not be significant.

3.5 Lessons Learned from the Electrothermal Modelling

The experience with electrothermal modelling has provided a few valuable conclusions regarding what would be the best practices to adopt in terms of any future modelling necessary to be included in a future on-line health monitoring system. The main points are:

- A model is only as good as the parameters defining it. Thus, there are no perfectly accurate models, since it is impossible to account for all real-life variables that may be influencing the modelled system.
- This is especially true for general "learning" type of models as the ones attempted at this stage of the project work. For example, it would be hard to know whether a given power loss estimate obtained form an inverter model is correct – it would be correct for such electrical system with exactly the same control scheme or filtering arrangements as used in the model, but whether or not such a system exists is another question. One may ask – why not then try to model a specific converter. The answer to this is that such a model could be made for lab converters perhaps, but the amount of complexity involved into an industrial converter such as the ones

used in offshore wind turbines and the fact that no manufacturer would openly give out all their design information (especially for converters currently on the market and generating revenue for them), means that such a modelling is really outside the scope of most academic research project. And in terms of the specific topic of this project, going into too detailed converter modelling can be considered a deviation.

- Therefore the use of such models here does not aim to yield results machining existing real-life data, nor to predict such data, but mainly to develop a better idea of what the working semiconductor devices would be experiencing inside a converter.

- It was found that maths and logics based simplification (i.e. using a maths function to create a waveform, instead of simulating the operation of circuits of electrical elements to obtain this waveform form there) is full justifiable in the light of the above discussion, as it yields similarly accurate results as the models based on electrical circuits, but optimises the running of the model dramatically.

- In the case of thermal models, the main findings that Foster and Cauer networks are already simplifications, especially the Foster networks which have no correlation to the physical structure of the system and should only be used to model a complete heat flow path, as addition of extra elements (e.g. adding a heat sink resistance and capacitance to a model which only describes the junction to case heat flow path) will render their results incorrect. In the physics based Cauer models, such additions are possible. However, paralleling any of the lumped element models (e.g. to describe systems with more than one heat source) is not recommended as it can produce significant errors. The explorative modelling exercises with Cauer

networks have established that summing all identified thermal resistances together in one lump R_{th} value for the system still produces valid steady state results and can be accepted as another useful simplification for improving the run time of the model.

Chapter

4 Reliability Issues Arising from Paralleling Chips

The paralleling of semiconductor chips is a common feature in modern power modules. It allows higher current conduction capabilities, but it also poses the potential problem of unequal current sharing between the paralleled devices. Packaging degradation is one of the factors that can causes unequal current sharing. This chapter presents an electro-thermal model which investigates the effects of non-uniform module degradation affecting the operation of parallel chips of the same kind and the same packaging. The focus is predominantly on press-pack devices where this non-uniform degradation usually manifests as differences in the clamping pressure of chips in central and edge positions, arising over time. The loss of pressure experienced by some of the chips depending on their positions leads to the increase of their contact electrical and thermal resistances and to the unequal current sharing amongst the parallel devices. Non-uniform degradation in

standard DBC modules can also lead to unequal current sharing between parallel devices.

4.1 Problems with Parallel Devices

In applications where parallel connection of multiple devices is required for high current conduction capability, maintaining electrothermal uniformity between chips is important. This is because current focalisation can lead to thermal runaway. For example, a wire bond lift-off resulting from thermo-mechanical stress cycling can increase the on-state electrical resistance of one parallel power device while not affecting another. Thus the parallel devices will have different electrical resistances and will not therefore share current equally and this will also lead to different heating of the devices. Likewise, non-uniform degradation in the solder die attach will cause differences in the thermal resistance of the power devices and their different junction temperature will affect the mobility of charge carriers in each chip and thus result in different current conduction capability.

In press-pack technology, non-uniform degradation can have even more pronounced effects as one of their major reliability concerns is the loss of pressure uniformity, which is a particularly important consideration for IGBT applications. Unlike thyristor wafers, IGBT press-pack power modules contain multiple parallel power devices subjected either to a global clamping force or individual spring contacts, depending on the design, and it has been observed in such modules that often edge located devices are exhibiting gradually reducing contact pressures

compared to centre located devices [78]. Loss of pressure uniformity results in chip-to-chip variation in both the junction-to-case thermal resistance and the on-state electrical resistance. In press-pack modules, the thermal and electrical resistance are inextricably linked together as both are dependent on the contact provided by the clamping forces [85]. As a result of the non-uniform pressure is in press-pack modules there will be a pronounced chip-to-chip variation in junction temperature, which depending on the temperature coefficient of the power semiconductor, can result in electrothermal convergence (stable current sharing) or electrothermal divergence (thermal runaway due to current focalisation). Critical to the current sharing stability of the module is the zero-temperature-coefficient (ZTC) in the forward characteristics of its power devices.

4.2 Significance of ZTC in Paralleling

The zero-temperature coefficient (ZTC) point of a power device is the point at which its electrical characteristics are invariant with temperature. Below this point, for the same on-state voltage, current will increase with temperature as a result of increased intrinsic carrier concentration. Above it, current will decrease with temperature as a result of increased on-state resistance and deteriorated mobility of the charge carriers. Power modules are stable for currents above the ZTC point since the forward voltage (and thus the on-state resistance) increases with temperature and the increased instantaneous power dissipation (heat) causes the current to reduce according to the current divider rule. For currents below the

ZTC point, the forward voltage reduces with increasing temperature meaning that the hotter device becomes less resistive thereby able to conduct more and more current. Hence in the context of paralleling multiple devices, it is desirable that their ZTC point is positioned low on their characteristic $V_f - I_f$ curve and that they operate at current levels above this point.

4.3 Electrothermal Model of Parallel Diodes

A Simulink model was developed to study the effects of electro-thermal non-uniformity in parallel diode chips with special focus on the current sharing between them. The model's basic electrical circuit is illustrated by Figure 34. It consists of two diode chips connected in parallel and a source providing the current flowing through them. If the chips are the same (of the same electrical and physical characteristics, same brand, rating, packaging, ect.) the current will be equally divided between the two. The two diodes are also expected to have the same thermal behaviour.

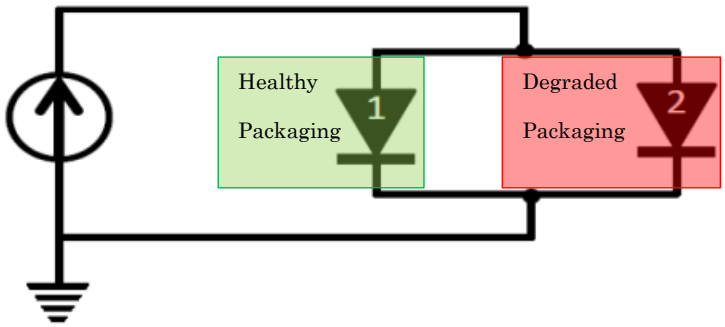


Figure 34. Basic electrical circuit used in the parallel diode electrothermal model with device 1 experiencing the effects of healthy packaging and device 2 experiencing effects of packaging degradation.

However, if one of those diodes has a slightly increased electrical and/or thermal resistance in comparison with the other one, this will not be the case. Although the chips themselves are manufactured to be electrically identical, degradtion of the packaging often leads to such non-uniformity. In press-packs where degradtion usually means reduction or loss of contact pressure, this will manifest as deterioration of both the electrical and thermal contact resistances. This creates a complicated scenario as the affected devices are likely to conduct a smaller share of the current but at the same time operate at higher T_j than expected for the level of current they conduct – with the T_j and the current through the device constantly influencing one another.

So the aim of the model is to study the net effect from such non-uniform current sharing and T_j. We are interested to see whether the parallel diodes will experince some sort of self-stabilisation of current and temperature resulting from

larger portion of the current being diverted to the non-degraded device while the degraded one conducts less slowing down its degradation in time, or whether the degraded device will take progressively more current as it heats up resulting in a thermal runaway and increasingly speeded degradation process.

Five different diodes of very similar electrical rating were examined via this modelling process. Table 7 below lists the devices modelled.

Table 7. Diode chips used in the parallel diode model

	Brand	Part Number	Technology	ZTC Current
	Cree	CPW5-1200-Z050B	SiC - Schottky	8.5 A
	ABB	5SLY 12E1200	Si - PiN	46.8 A
	Infineon	SIDC42D120E6	Si - PiN	27 A
	Semikron	SKCD3C120I4F	Si - PiN	56 A
	Vishay	VS340DM12Cx	Si - PiN	132 A

Their brand will be used as shorter notation for referring to them further on in this text. The rated current of these diodes is 50A.

The modelling concept used is the same as the one of the electrothermal models described in the previous chapter – i.e. their electrical and thermal behaviour are modelled alongside each other in a feed-back loop.

4.3.1 Thermal part of the model

The thermal model is extracted as a Cauer network based on the dimensions and material physical properties of the elements of the thermal system – i.e. the chip and its packaging. The packaging chosen for the purposes of this model is based on a physical press-pack designed to house the Cree SiC chip [100] of which the exact part dimensions and materials were known. Figure 35 shows a cross-section of this press-pack. It consists of a copper base and top which provide paths for both the electrical current and the heat dissipation, molybdenum contact plates between which the chip sits and die carrier which represents a plastic casing that ensures the alignment of the diode chip and the molybdenum plates.

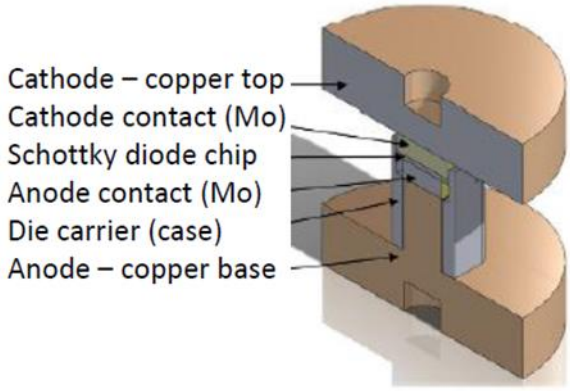


Figure 35. Press-pack used as a basis for the thermal model [100].

For the modelling of the Cree diode, the packaging dimensions used for estimating the thermal resistance and capacitance of the system are exactly the

ones of the real press-pack. For the modelling of the other four silicon chips, the same packaging concept and the same outer packaging dimensions are used, but the contact surface areas of the molybdenum plates and the copper pedestal of the anode base are adjusted according to the relevant chip surface area.

For simplicity the thermal system in this model is defined only from junction to case. The heat sink or cooling is assumed to be ideal and able to maintain 25 ° C at the outer surface of the packaging. Since some previous experiments have been carried out with single side cooling (anode side cooling), the model also reflects only single side cooling (as experiments carried out with this press-pack also used single side cooling).

The extraction of the Cauer thermal resistance (R_{th}) and thermal capacitance (C_{th}) values which correspond to the different physical material layers of the packaged device was done following previously described procedures [39], [101]. The result was a 4^{th} order Cauer network with stages corresponding to the chip, the anode molybdenum layer, the anode copper contact pedestal and the copper contact base. An example calculation of these values for the Cree SiC Schottky diode is presented in Table 8.

Table 8. Cauer network R_{th} and C_{th} value extraction for the Cree diode press-pack.

Material layer	Area=l·w A (m^2)	Thickness d (m)	Volume V (m^3)	Heat conductivity k (°mK)	Heat storage s (Ws/Km^3)	Thermal resistance R_{th} = d/(kA) (K/W)	Thermal capacitance C_{th} = sV (Ws/K)
SiC chip/2	2.401E-05	0.0002	4.562E-09	380	2214900	0.0208	0.010
anode Mo	1.348E-05	0.0015	2.022E-08	138	2217740	0.8063	0.045
Pedestal (anode)	1.296E-05	0.006	7.776E-08	394	3400000	1.1750	0.264
Base (anode)	0.0002739	0.005	1.394E-06	394	3400000	0.0463	4.738
JUNCTION TO CASE – Total R_{th}						2.0485	

The Cauer ladder was further simplified to just one R_{th}-C_{th} rung, by adding all thermal resistances in one sum total value and finding a C_{th} value for which the step input response of the simplified ladder sufficiently approximates the response of the higher order network. We are interested in steady state current sharing and in steady state operation, once the thermal capacitances of the system are saturated only the thermal resistances in series impede the heat flow, therefore such simplification is justified.

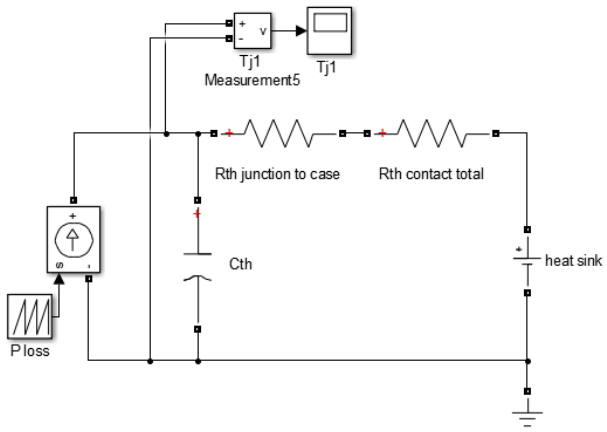


Figure 36. Simplified thermal model used in the electrothermal simulation of the parallel diodes.

Figure 36 illustrates the simplified version of the model obtained by summing the different layers' thermal resistances from 4th order Cauer network. Since this is a press-pack, apart from the material thermal resistance there also is pressure-dependent contact thermal resistance (normally modelled as additional resistance added in series with the material thermal resistance of the corresponding material layer). Determining contact thermal resistance is usually done experimentally as it depends on a number of different factors such as the contacting materials, the surface roughness and clamping pressure. For the purposes of this model an indicative value for the contact thermal resistance of the non-degraded device was obtained from data presented in a paper on experimental determination of contact resistances in press-packs [102]. It is almost negligible in comparison with the material thermal resistance for higher clamping pressures.

For the purposes of the modelling of the different diodes, here we make the following assumptions:

- the packaging materials for all diodes are the same;
- the corresponding packaging layers have the same surface roughness;
- thus, the clamping pressure is the only factor affecting the contact thermal resistances;
- the contact thermal resistances can be added together and modelled as one lump sum resistance in series with the total thermal resistance of the packaging materials.

Based on the earlier published experiments with the Cree chip press-pack [103], the pressure resultant from a clamping force of 500 N is taken to be the normal clamping pressure (approximately 20.8 MPa) and the pressure resultant from a clamping force of 300 N is taken to represent reduced pressure after degradation (approximately 12.5 MPa). Figure 37 published in [86] shows that this difference in pressure results (about 7% increase of the total R_{th}).

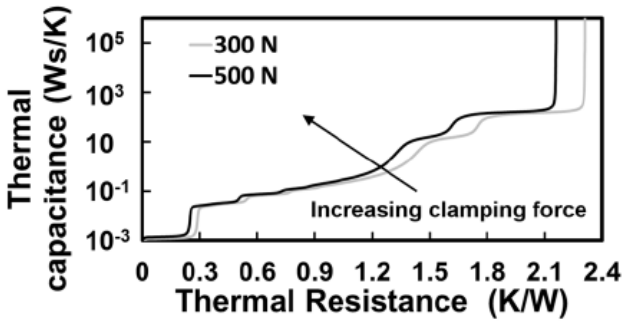


Figure 37. Effect of the change of clamping force on the press-pack's thermal resistance [86].

In the parallel diode electrothermal models here the same percentage increase of thermal resistance is used as added contact thermal resistance for the degraded device. Following the assumptions stated above, if the pressure is the only factor affecting the contact thermal resistance and we use the same the normal and reduced clamping pressure levels consistently, then the percentage rise of the total thermal resistance for all different brands modelled should also be the same.

Thus the thermal models of the two diodes in parallel – one with normal and one with degraded packaging – will have the same thermal capacitance and material thermal resistance, but different contact resistances. The degraded device's contact thermal resistance will be equal to 7% of the total thermal resistance of the non-degraded device or around 0.14 K/W.

The total thermal resistance calculated following the above method for the non-degraded case of the Cree press-pack – around 2 K/W – may seem large, but

it is very close to thermal resistance value experimentally measured for this press-pack in [100], which gives confidence that thermal modelling yields reasonable values.

In press-packs, the loss of pressure is coupled with increase of electrical resistance as well as thermal resistance. This is confirmed by [86] through experimental measurements with the Cree diode press-pack. This paper also gives an average value for the increase of the electrical contact resistance resulting from the mentioned pressure loss and shows that current sharing will still be uneven even at cold start when the junction temperatures of the two devices is the same (as the ambient).

To reflect this in the parallel diode models, the mentioned experimentally derived contact resistance value is added as a bias to the on-state resistance of the degraded device (with packaging pressure-loss). The on-state resistance is dependent on the current and junction temperature, so it is continuously recalculated and updated by the model, in a feed-back loop with the other two parameters.

4.3.2 Electrical part of the model

For the electrical part of the model, the manufacturer's datasheets are used to extract in the form of a 2D Look-up tables (LUT) the relationship between the forward voltage V_f, current I_f and junction temperature T_j. The model is interested

in establishing the current sharing between devices, therefore it considers their on-state only.

The electrical model for power loss estimation of the parallel diodes was first developed using simulated electrical and electronic components – i.e. controlled current source and two diodes in parallel with some extra resistive branches to stabilise the circuit – as shown in Figure 38.

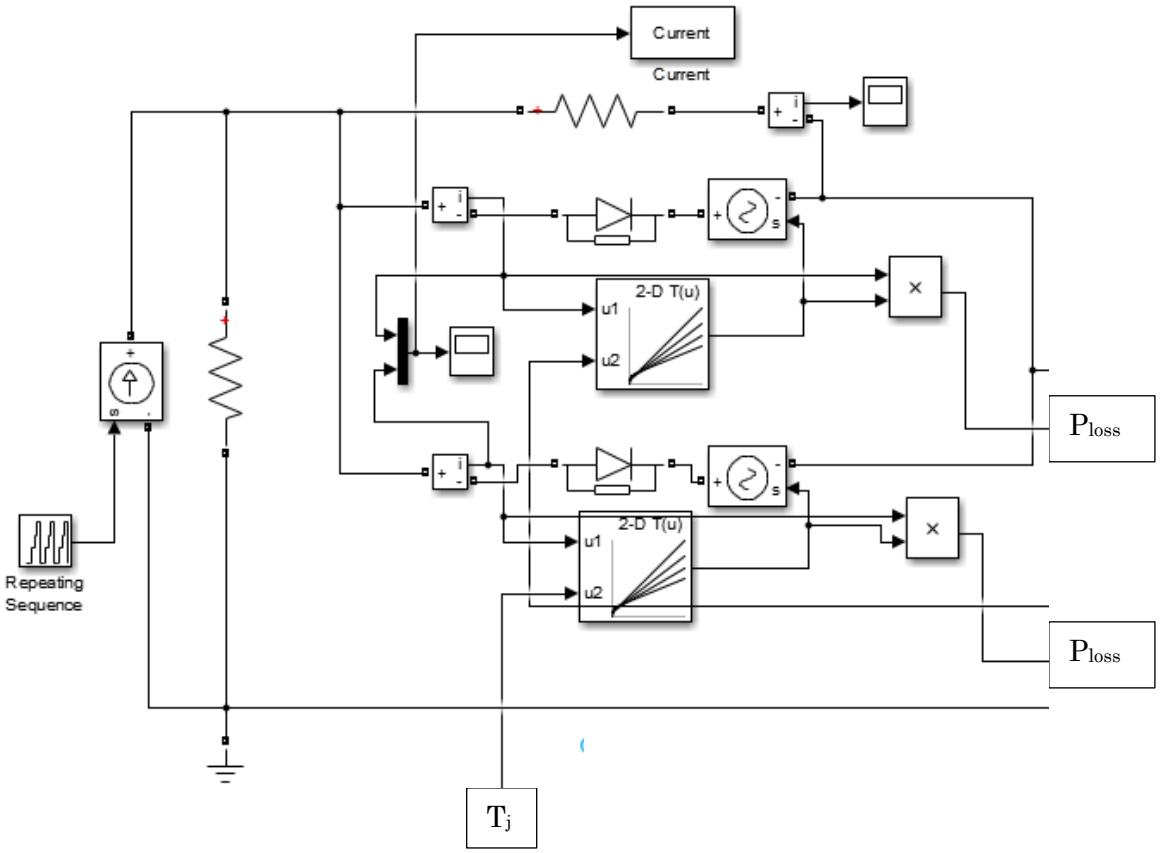


Figure 38. Electrical power loss model for parallel diodes using LUTs to derive their forward voltage drop which is then used in the conduction power loss calculation.

However, the electrical model was running slowly and encountering simulation problems and again it was found that a mathematical simplification provides the same results while significantly optimising the model run-time. Figure 39 below illustrates the simplified maths-based model flowchart showing how the current and temperature are being updated in a feed-back process. It is important to note that the electrical resistance of the opposite device determines the proportion of current carried –according to the current divider rule.

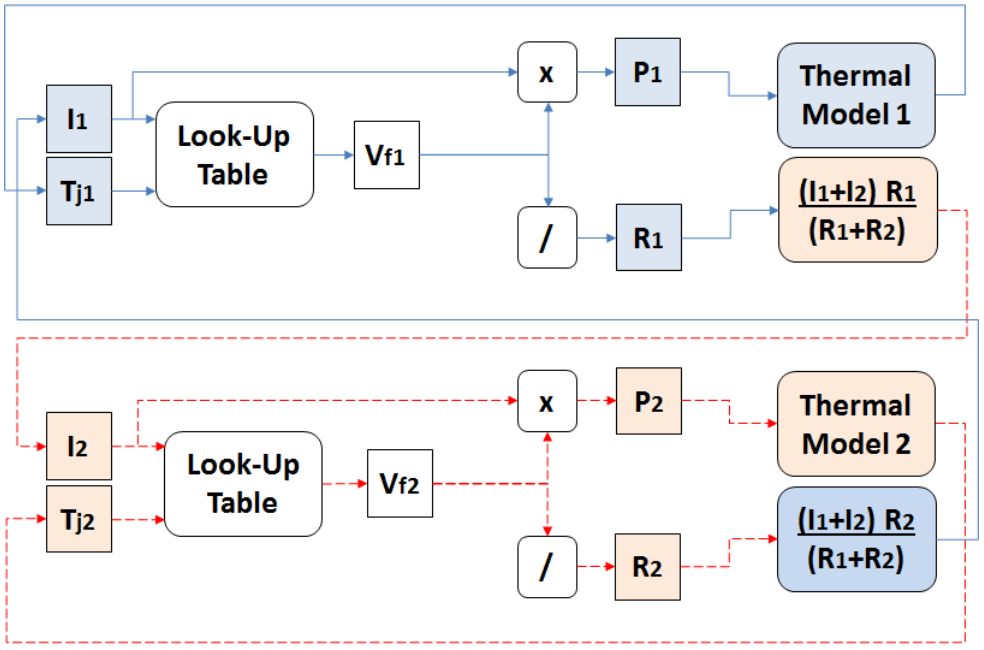


Figure 39. Simplified parallel diode electrothermal model flowchart.

The complete electrothermal model algorithm is as follows:

1. Initial current and temperature values are supplied to start the first model iteration.

2. They are fed into the diodes I_f-V_f LUT producing a value for the on-state voltage.

3. This voltage value is used together with the current to calculate the on-state resistance of each diode and its power loss.

4. The power loss P of each device is used to calculate what its own T_j will be at the next iteration.

5. The resistance R of each device is used following the current divider rule to determine how the current splits at the next iteration. The current through each device is proportional to the resistance of the opposite device.

This model was used with LUTs for each of the 5 diodes technologies listed above at a few different current levels, aiming to illustrate their current sharing behaviour in operation below, above and at the ZTC point. The results are presented in the following section.

4.4 Results from the Parallel Diode Model

4.4.1 Results with 10A total current

The following graphs (Figure 40 – Figure 44) present the current sharing and junction temperature of the parallel diodes modelled at a total current of 10A,

which split between the two parallel devices should result in 5A through each of them. At this current level all the modelled diode brands are operating below their ZTC point. It can be seen that in all 5 cases the healthy device takes a larger share of the current, although both devices are operating at very similar junction temperatures. This is due to the higher electrical resistance of the degraded device. Also at such low current (in comparison to the rated diode current of 50A), the temperature effects are not yet prominent.

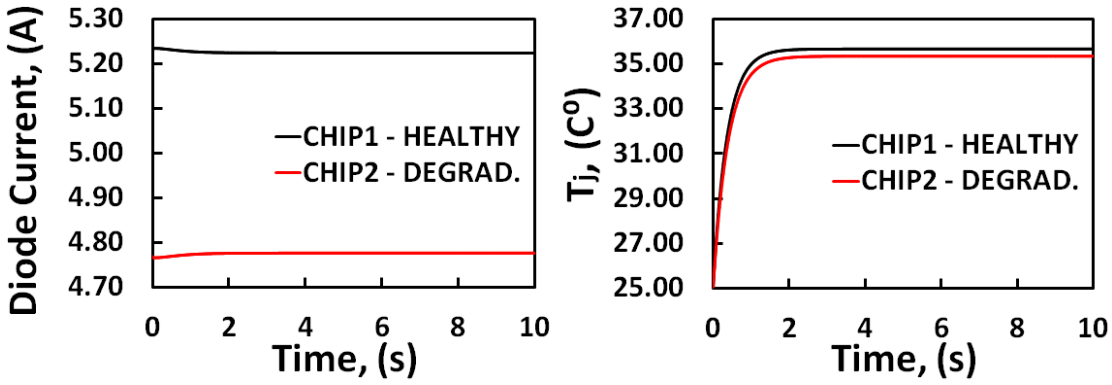


Figure 40. Cree SiC Schottky diodes: current sharing and junction temperature obtained from the parallel diode model at 10A total current.

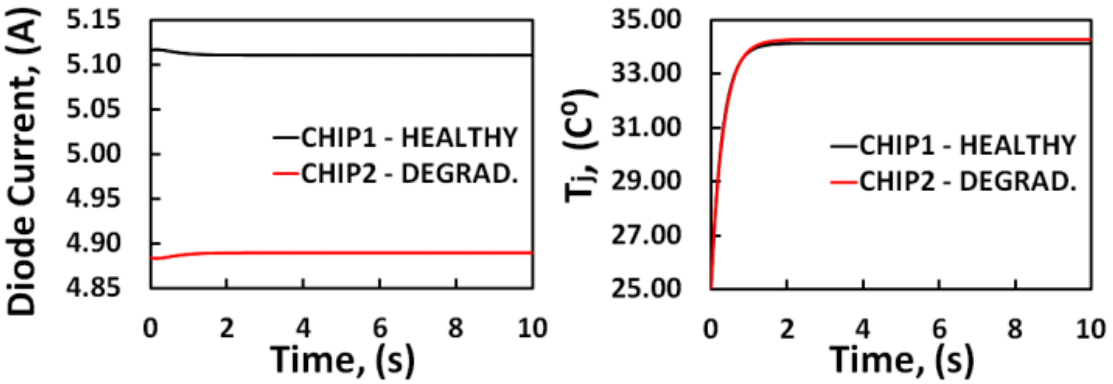


Figure 41. Infineon diodes: current sharing at and junction temperature obtained from parallel diode model at 10A total current.

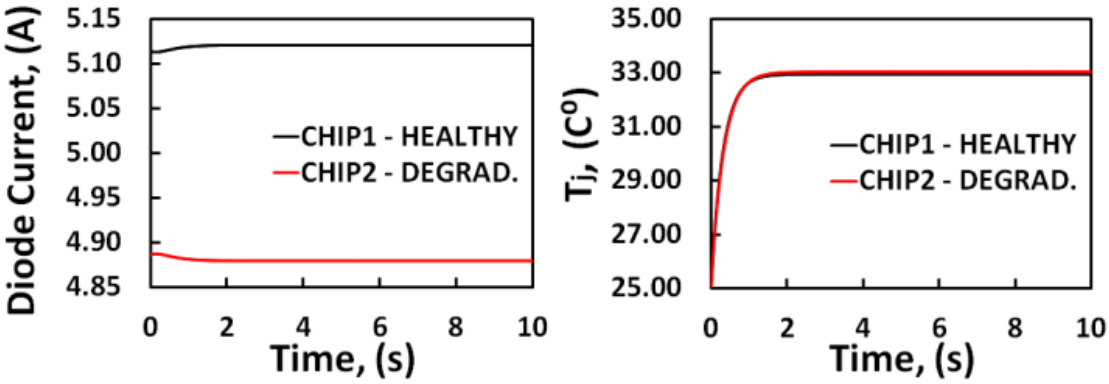


Figure 42. ABB diodes: current sharing at and junction temperature obtained from parallel diode model at 10A total current.

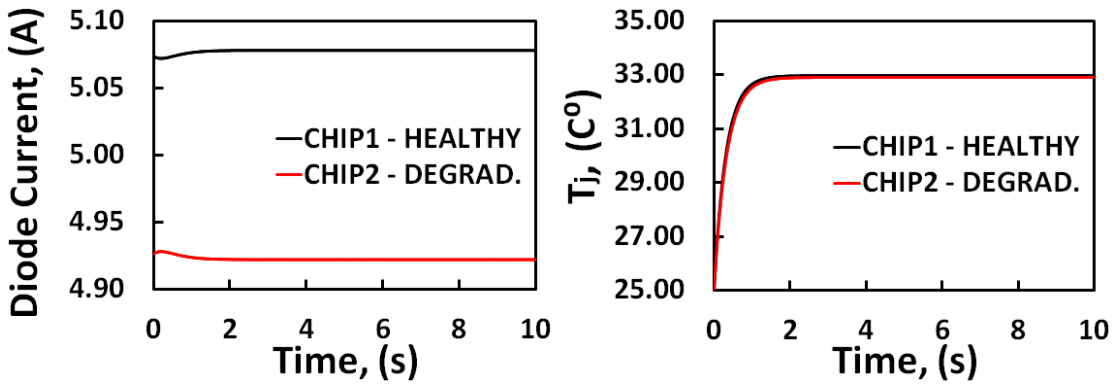


Figure 43. Semikron diodes: current sharing at and junction temperature obtained from parallel diode model at 10A total current.

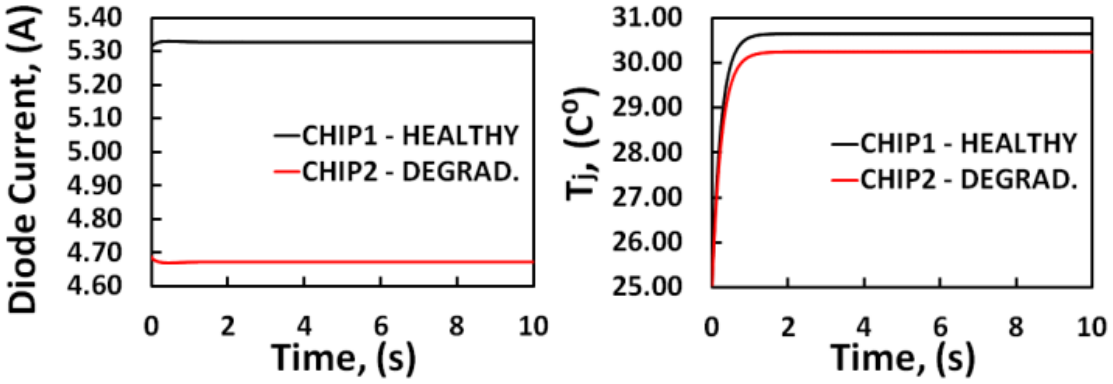


Figure 44. Vishay diodes: current sharing at and junction temperature obtained from parallel diode model at 10A total current.

4.4.2 Results with 20A total current

The following graphs (Figure 45 – Figure 49) present the current sharing and Junction temperature of the parallel diodes modelled at a total current of 20A, which split between the two parallel devices, should result in 10A through each of

them. At this current level the Cree diode operates above its ZTC point while all other modelled diode brands still operate below theirs.

Again, it can be seen in all instances that the influence of the electrical resistances outweighs that of the thermal resistance, but in the case of the Vishay diodes the effect of the heating on the increase of current becomes more visible now.

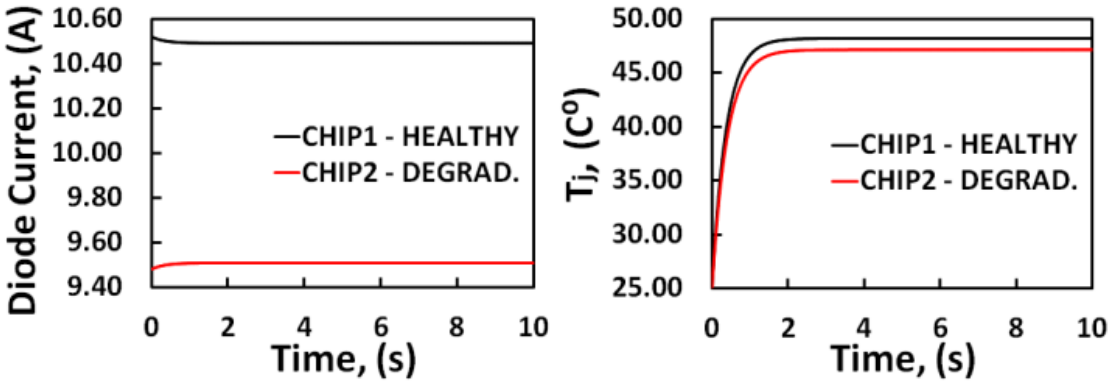


Figure 45. Cree SiC Schottky diodes: current sharing at and junction temperature obtained from parallel diode model at 20A total current.

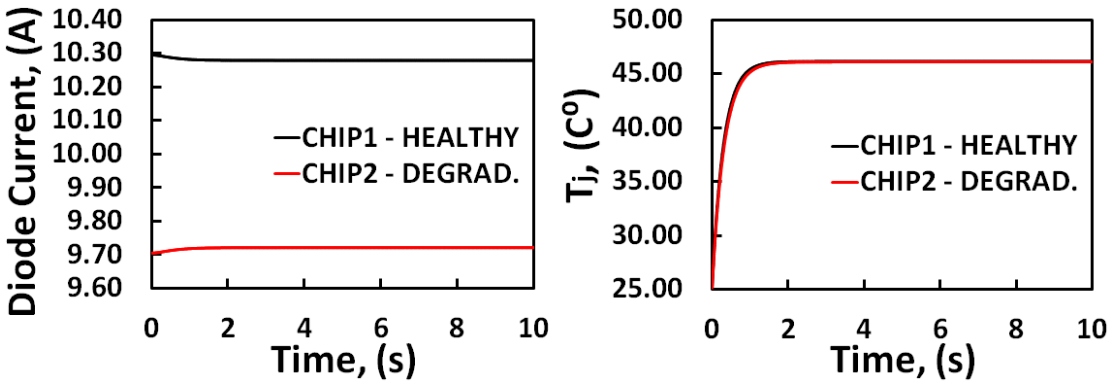


Figure 46. Infineon diodes: current sharing at and junction temperature obtained from parallel diode model at 20A total current.

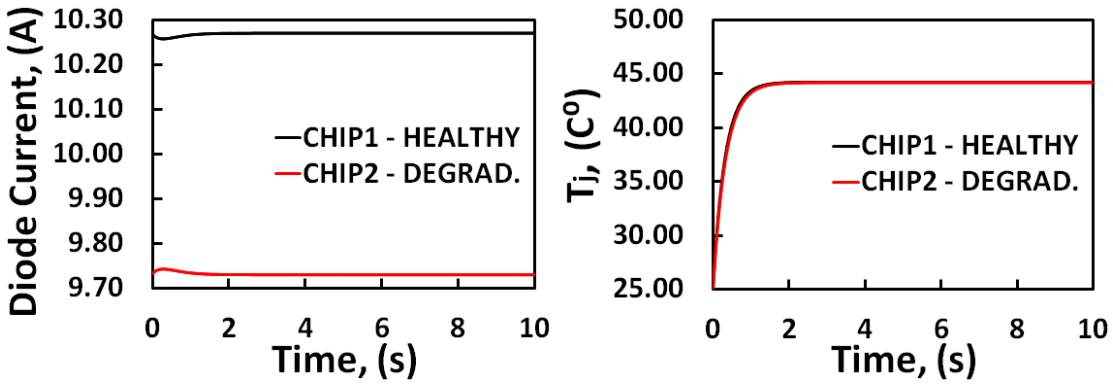


Figure 47. ABB diodes: current sharing at and junction temperature obtained from parallel diode model at 20A total current.

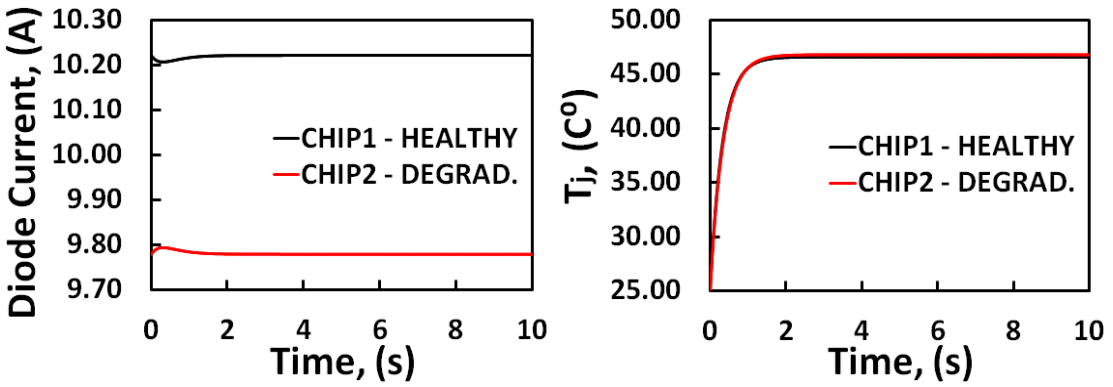


Figure 48. Semikron diodes: current sharing at and junction temperature obtained from parallel diode model at 20A total current.

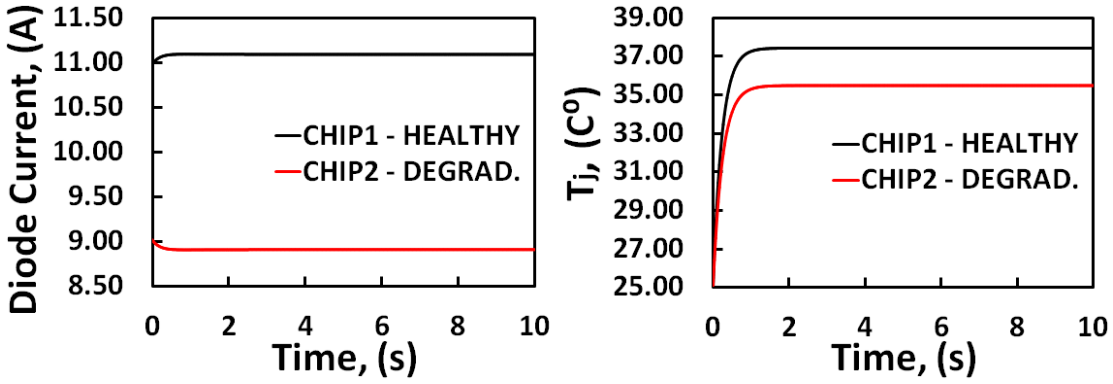


Figure 49. Vishay diodes: current sharing at and junction temperature obtained from parallel diode model at 20A total current.

4.4.3 Results with 40A total current

The following graphs (Figure 50 – Figure 54) present the current sharing and Junction temperature of the parallel diodes modelled at a total current of 40A, which split between the two parallel devices, should result in 20A through each of

them. As previously at this current level the Cree diode operates above its ZTC point while all other modelled diode brands still operate below theirs.

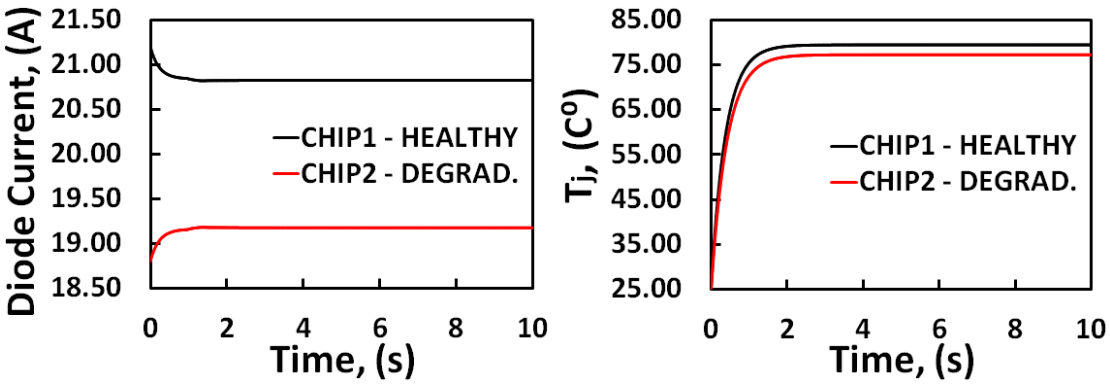


Figure 50. Cree SiC Schottky diodes: current sharing at and junction temperature obtained from parallel diode model at 40A total current.

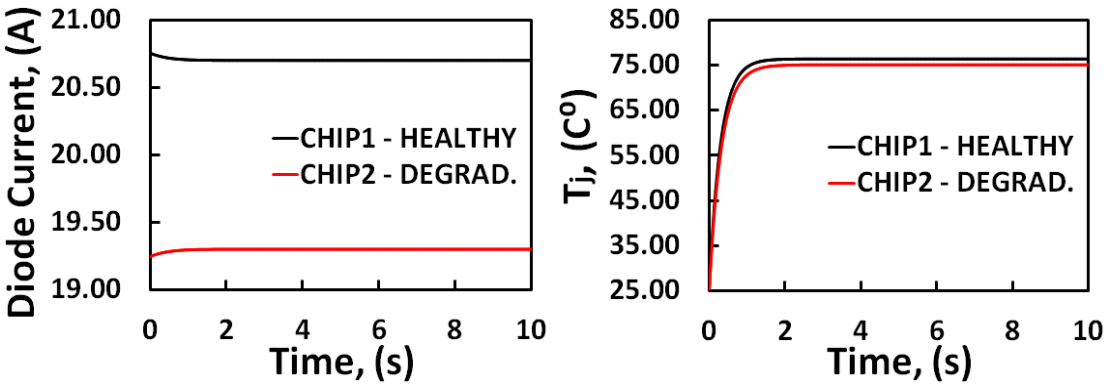


Figure 51. Infineon diodes: current sharing at and junction temperature obtained from parallel diode model at 40A total current.

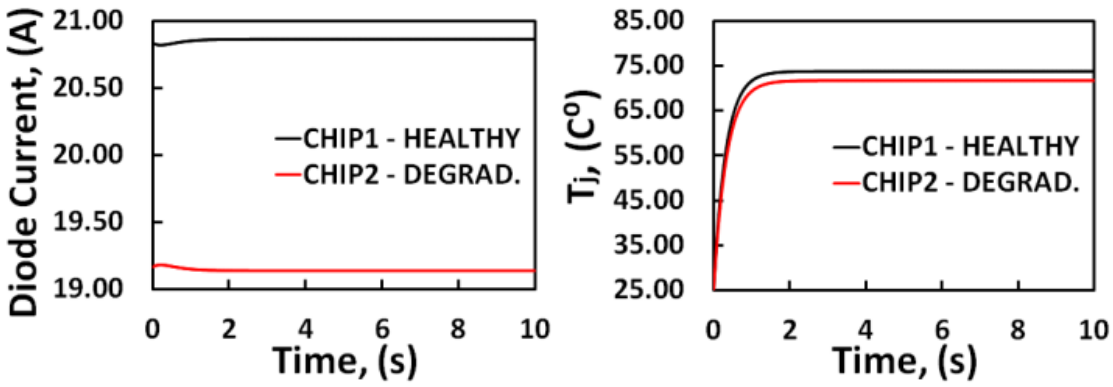


Figure 52. ABB diodes: current sharing at and junction temperature obtained from parallel diode model at 40A total current.

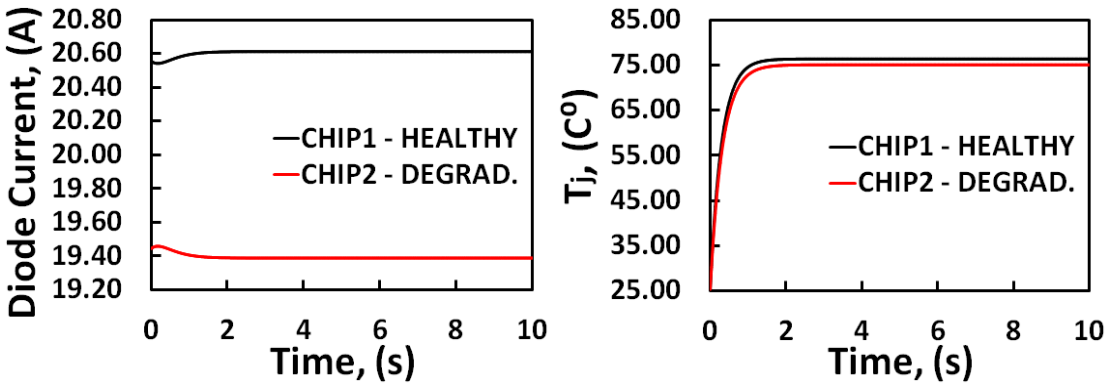


Figure 53. Semikron diodes: current sharing at and junction temperature obtained from parallel diode model at 40A total current.

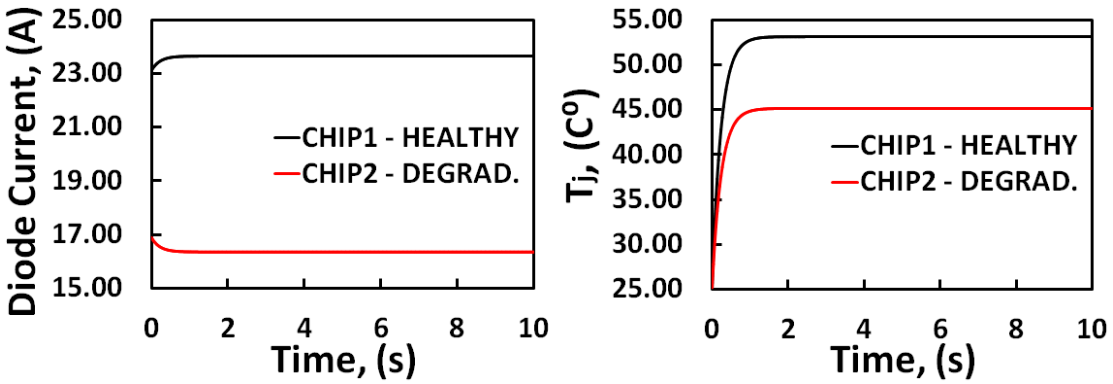


Figure 54. Vishay diodes: current sharing at and junction temperature obtained from parallel diode model at 40A total current.

4.4.4 Results with 60A total current

The following graphs (Figure 55 – Figure 59) present the current sharing and Junction temperature of the parallel diodes modelled at a total current of 60A, which split between the two parallel devices, should result in 30A through each of them. At this current level the Cree and the Infineon diodes operate above their ZTC points, all other modelled diode brands still operate below theirs.

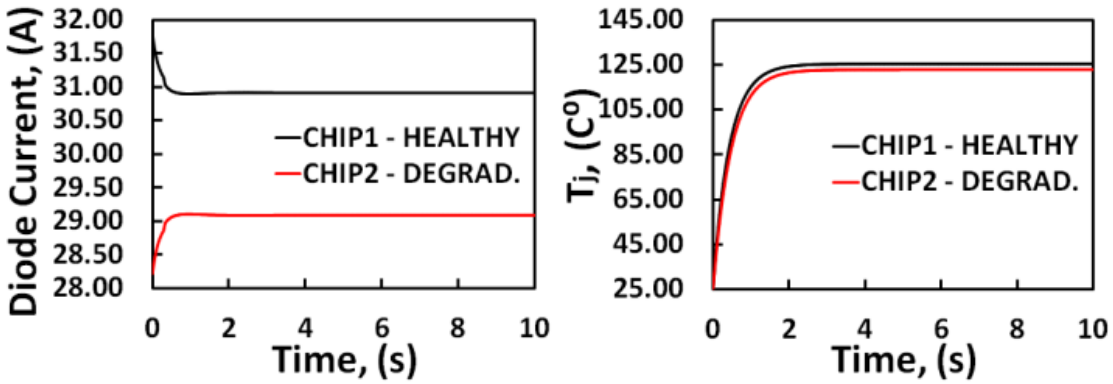


Figure 55. Cree SiC Schottky diodes: current sharing at and junction temperature obtained from parallel diode model at 60A total current.

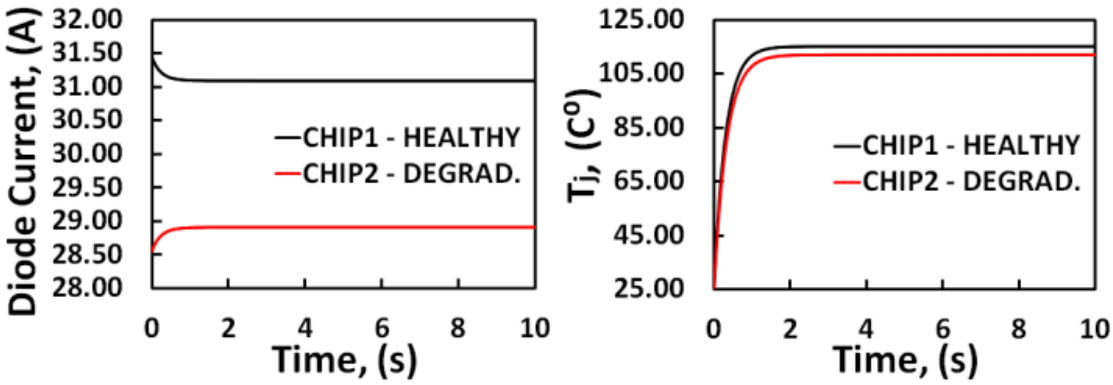


Figure 56. Infineon diodes: current sharing at and junction temperature obtained from parallel diode model at 60A total current.

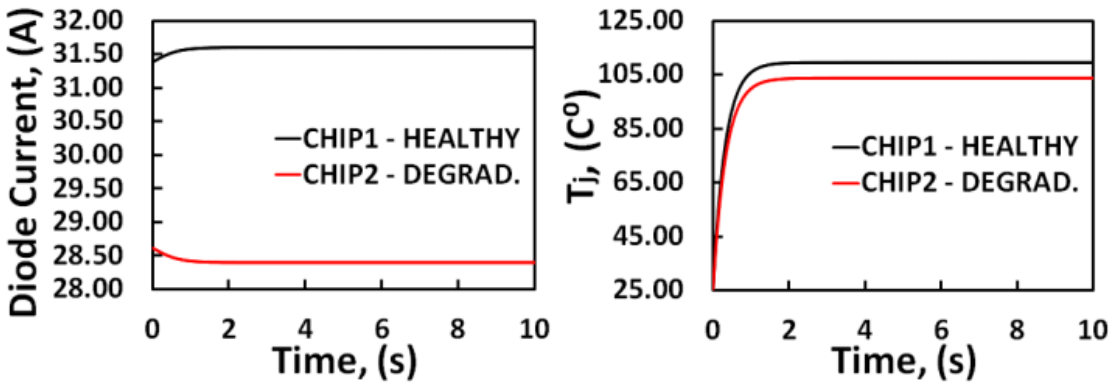


Figure 57. ABB diodes: current sharing at and junction temperature obtained from parallel diode model at 60A total current.

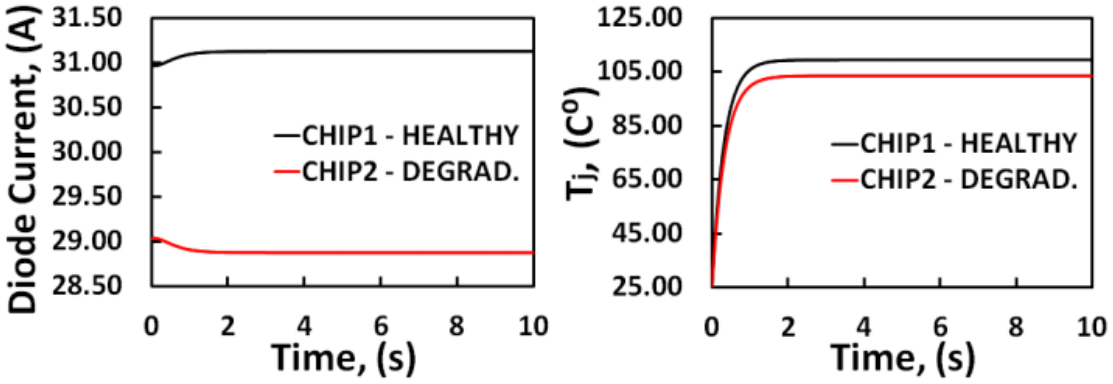


Figure 58. Semikron diodes: current sharing at and junction temperature obtained from parallel diode model at 60A total current.

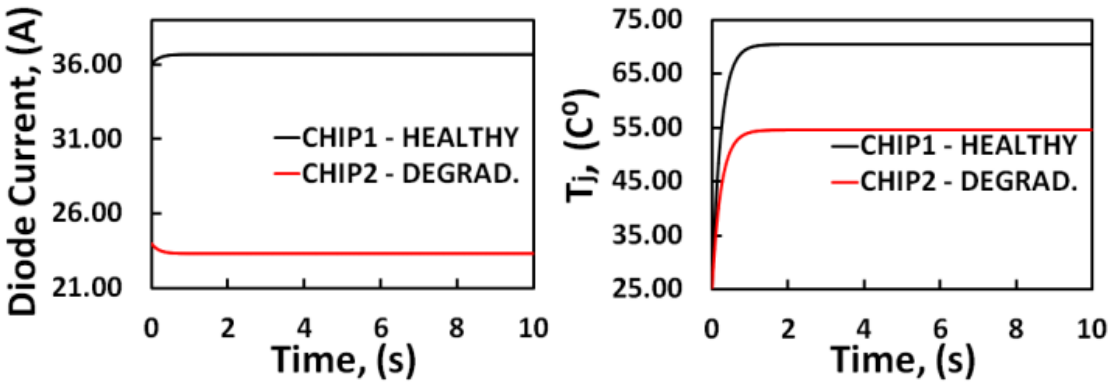


Figure 59 Vishay diodes: current sharing at and junction temperature obtained from parallel diode model at 60A total current.

4.4.5 Results with 80A total current

The following graphs (Figure 60 – Figure 64) present the current sharing and Junction temperature of the parallel diodes modelled at a total current of 80A, which split between the two parallel devices, should result in 40A through each of them. At this current level the Cree and the Infineon diodes operate above their ZTC points, all other modelled diode brands still operate below theirs.

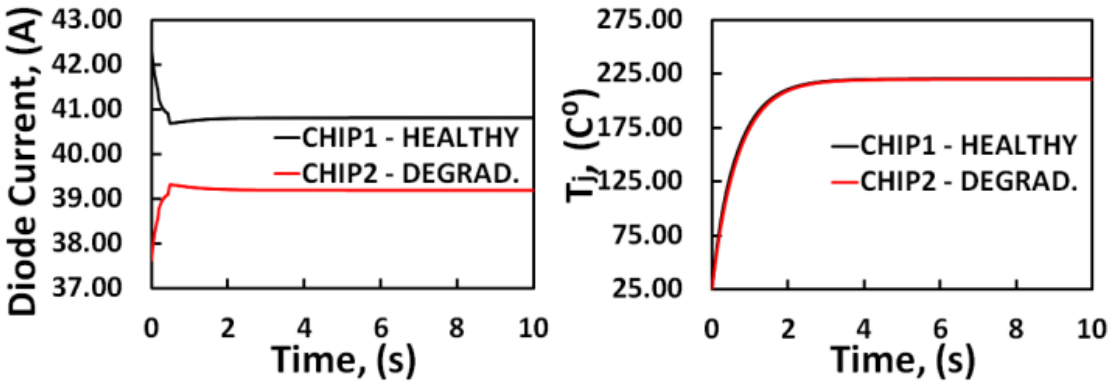


Figure 60. Cree SiC Schottky diodes: current sharing at and junction temperature obtained from parallel diode model at 80A total current.

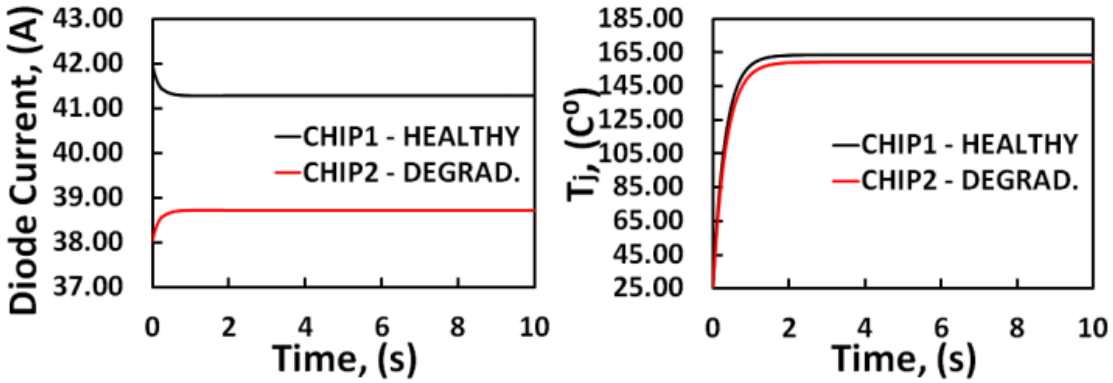


Figure 61. Infineon diodes: current sharing at and junction temperature obtained from parallel diode model at 80A total current.

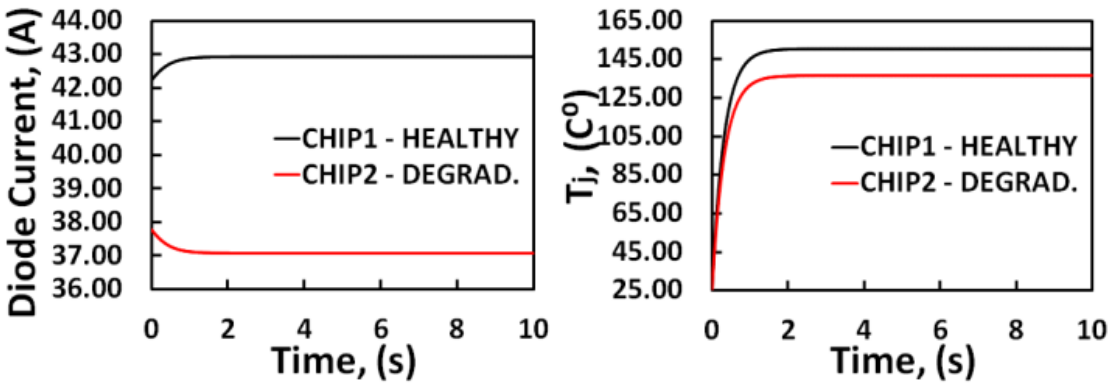


Figure 62.ABB diodes: current sharing at and junction temperature obtained from parallel diode model at 80A total current.

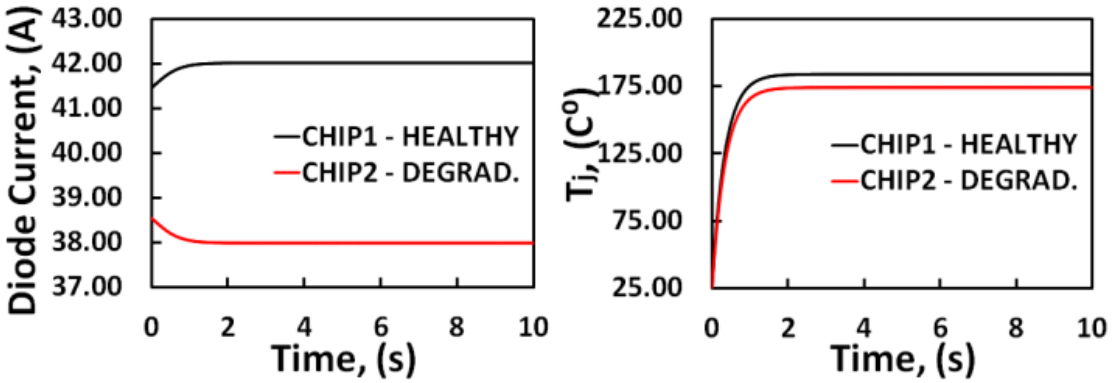


Figure 63 Semikron diodes: current sharing at and junction temperature obtained from parallel diode model at 80A total current.

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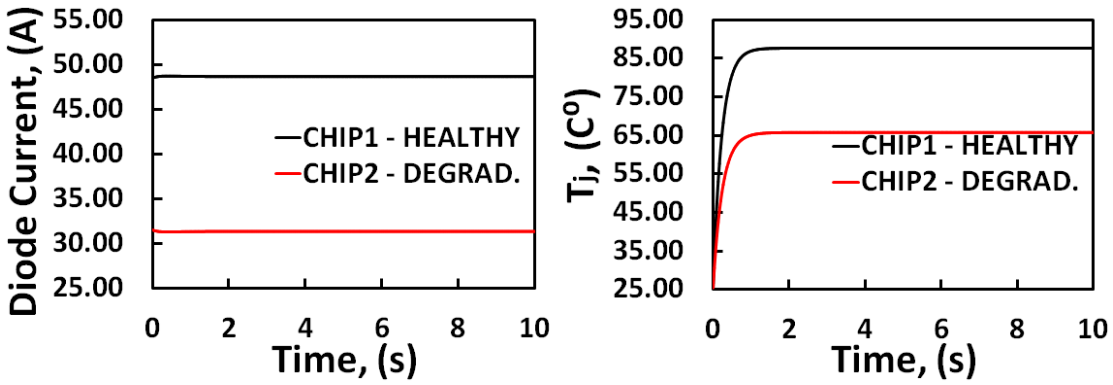


Figure 64. Vishay diodes: current sharing at and junction temperature obtained from parallel diode model at 80A total current.

4.5 Discussion of the Model Results

The results indicate that the current sharing between the chips is initially determined by the difference in their electrical resistance, but the subsequent the convergence or divergence of the current through the parallel devices also depends on the technology ZTC point. While the increase of electrical contact resistance due to partial pressure loss remains the dominant factor that determines how the current splits between the parallel devices, for higher current levels the devices operating above their ZTC point (Cree and Infineon) display a clear tendency towards convergence of both the current device and the junction temperature of the healthy and degraded device. Thus, a self-attenuating effect is achieved which does not allow increasingly larger amounts of current to be redirected into one device.

In PiN diodes with higher ZTC points, the opposite tendency can be observed: the already unequally shared current levels through the respective devices tend to

diverge still further with the increase of the total current. There is also a pronounced difference in the junction temperatures of the degraded and healthy devices – the degraded device has lower junction temperature, but this is not necessarily good news in the given scenario. As the device with non-compromised pressure contact is conducting more current in proportion it becomes hotter, its electrical on-state resistance decreases and allows it to conduct even more current, which makes it even hotter and more conductive – a vicious circle that can easily lead to a thermal runaway with destructive result.

Figure 65 below summarises the parallel diode modelling results for three of the examined chip technologies.

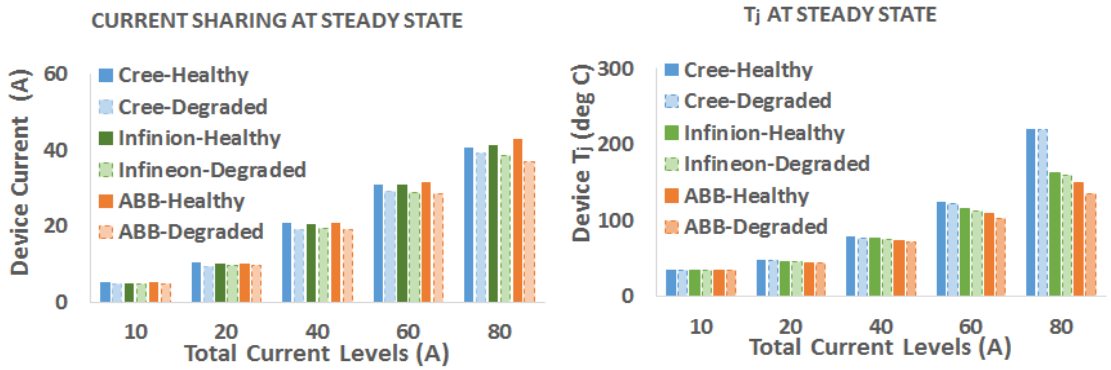


Figure 65. Parallel diode electrothermal modelling results summary.

The reason for the higher T_j levels of the Cree diodes at the highest modelled current level is not a flaw in the model. It is due to the small surface area of the

chip in comparison with the other diodes (resulting in higher thermal resistance for the same packaging) and the rise of its junction temperature is associated with higher rate of increase of the on-state voltage than observed amongst the other diode technologies. (Real life experiments were carried out on the Cree chip press-pack with maximum total current level of 40 A only.) Nevertheless, it can be seen that in press-packs paralleling devices with lower ZTC characteristic is better for maintaining current sharing stability and thermal equilibrium.

4.6 Parallel Devices in DBC Modules

In DBC modules, the main packaging degradation mechanisms as previously discussed are bond-wire lift-off which translates into increased electrical resistance and solder fatigue which translates into an increased thermal resistance. Unlike in press-packs where the loss of pressure leads to deterioration of both the electrical and the thermal contact and thus, to increase of both the electrical and the thermal resistances, in DBC modules these two types of resistance are not necessarily coupled together and the two degradation mechanisms mentioned above leading to their respective increase can manifest on their own. That is, the DBC module may experience only bond-wire lift-off without solder fatigue and vice versa.

The increased electrical resistance due to bond-wire lift-off will produce similar effect to the results of the press-pack models: the non-degraded device will carry more current which will make it hotter and depending on its ZTC – either more or less conductive as a result. Again, devices with low ZTC will benefit from

the fact that the hotter a device becomes, the higher its on-state resistance, which can help stabilise the amount of current it accepts, whereas the devices with high ZTC may tend to accept more current as they heat up. However, without the added influence of the increased R_{th}, the effect of the small increase of electrical resistance is going to be less pronounced than in the press-packs.

If on the other hand, one of the paralleled devices in a DBC module experiences increased thermal resistance due to fatigue in its individual die-attach solder layer, this will not affect its electrical resistance. The way the total current splits between a device with increased R_{th} and a device with normal R_{th} will depend only on their ZTC point with respect to the current they experience individually. Thus, if the total current is exactly twice the ZTC current of the devices they will share it equally and the increased R_{th} will have no effect on the sharing. The devices will still operate at different T_j – it will be higher for the degraded device. If the total current is lower than twice the ZTC current – the degraded device will both conduct a higher share of the current and operate at higher junction temperature than the healthy device. If the total current is higher than twice the ZTC current, then the degraded device will be carrying less current. It will still operate at higher T_j than the healthy device because of its increased R_{th}, but the fact that it will be carrying slightly less current will have an attenuating effect on its T_j.

Depending on how much the T_j affects the device's on-state resistance, the parallel device with higher R_{th} and operating below its ZTC point can suffer more

in a DBC module that in a press-pack. In press-pack the chip with increased thermal resistance also has increased electrical resistance meaning it will not be likely to go into a thermal runaway mode despite its increased junction temperature. The healthy device – i.e. the one without pressure loss is more likely to go into a thermal runaway there, if operating below its ZTC current. In a DBC module, however, it is the degraded device which will get hotter and with no added electrical resistance to protect it from taking more current, its own on-state resistance will decrease, allowing the passage of larger and larger portion of the currents which will further heat it and make it more conductive. Figure 66 and Figure 67 below illustrate this process.

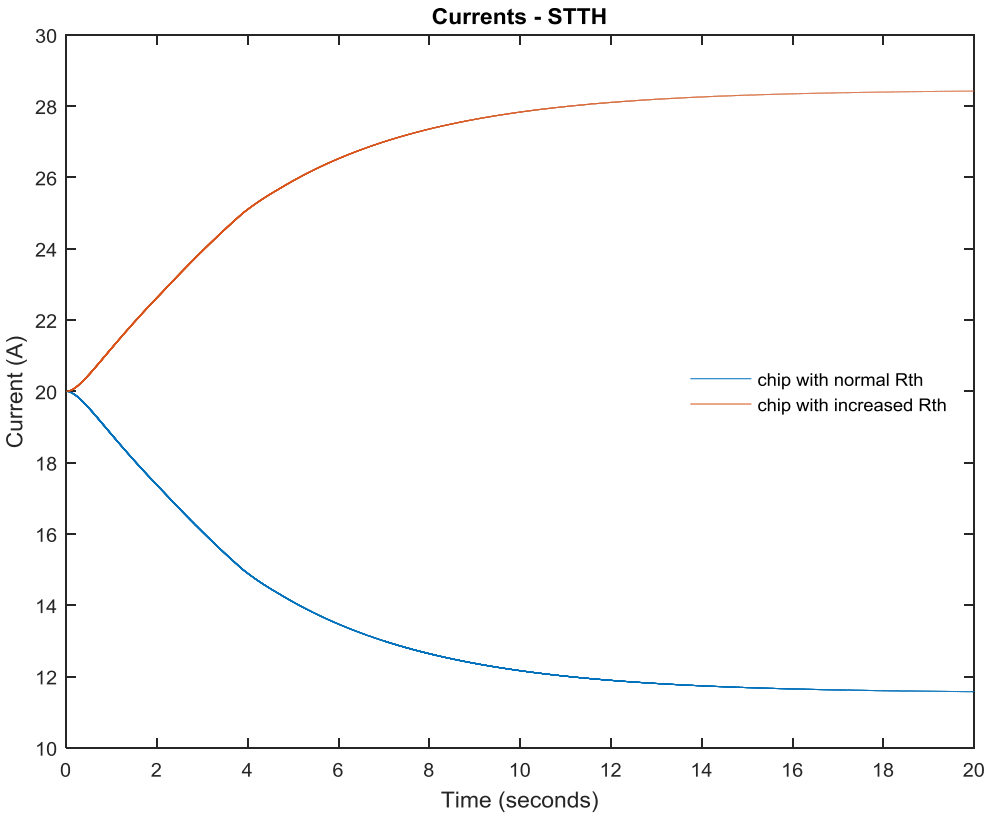


Figure 66. Current sharing result obtained from the parallel diode model using devices in standard packaging (STTH6012W).

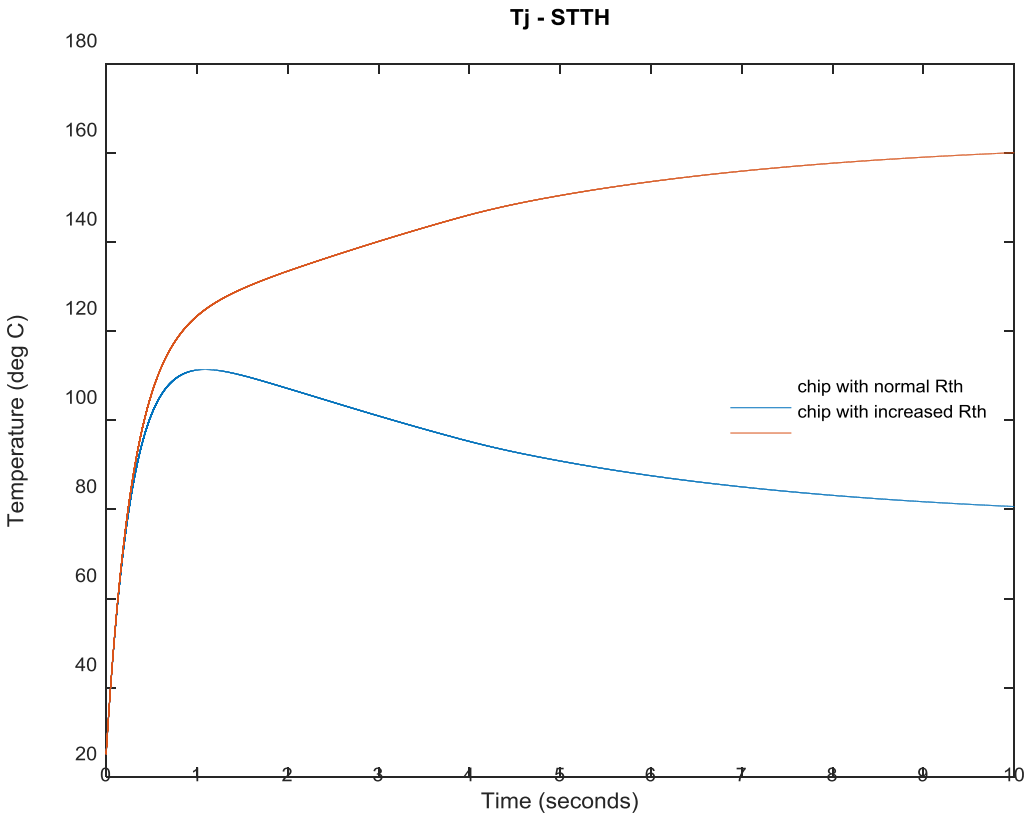


Figure 67. Junction temperature obtained from the parallel diode models using devices in standard packaging (STTH6012W).

Large DBC modules used in the converters of offshore wind turbines – such as the FF1000R17IE4 and the FF1000R17IE4D_2B – have 6 paralleled IGBT chips and 6 paralleled diode chips. The module's size is large and its cooling may not be uniform (e.g. if one part of the heat sink where the top half of the module is attached may be hotter another which cools the other half of the module). This means that it is likely that the die-attach solder layers inside will degrade at different rates; it is possible the solder in one part of the module will develop

delamination, while the rest of it remains more or less intact. Such effect of non-uniform degradation is something which a practical module health monitoring system will need to be able to recognise, as a module is considered degraded and should be replaced even if its degradation is only affects a small part of it. In the case of the IGBT chips which have low ZTC point and usually operate above it, this can mean that uneven increase of the individual chip junction-to-case R_{th} may be masked by the attenuating effect it has on their current sharing. However, this will also slow the degradation. The parallel diodes which have, in the case of the FF1000R17IE4D_2B module especially, ZTC point higher than the module's rated current – meaning they will normally operate below their ZTC – uneven degradation can be problematic. Nevertheless, spots with increased temperature on the module casing can point to such degradation in progress.

4.7 Conclusions

From a design point of view using devices which would normally operate below their ZTC current is beneficial in all cases where paralleling of individual chips is necessary for reaching higher current ratings. This will improve the current sharing amongst the parallel chips by diverting current from more degraded chip (i.e. easing its work load), lower the differences between their junction temperatures and generally work towards slowing the overall degradation rate of the module.

From the point of view of the power module's condition or health monitoring however, having parallel devices subjected to non-uniform packaging degradation can make it more difficult and complicated to detect, identify and monitor this process. Detection of excess heat spots that may come from devices operating below their ZTC current may be helpful in this respect. This would necessitate using more than one case temperature measurements for large modules with multiple paralleled chips and thermal model which will be able to interpret multiple case temperature inputs.

The use of multiple built-in thermal sensors might provide a reasonable solution to the monitoring of non-uniform degradation of power modules, although this would make the power module more complex in circuit structure and more expensive. Of course, this it may cause additional reliability issues as well.

Chapter

5 Die-attach Scans

So far the IGBT electro-thermal modelling provided a operation in a standard converter topology, its power losses and how degradation affects them. It is further necessary to take a look at the actual physical modules for which we are trying to find a health-monitoring solution. Since the focus of this work is on the solder fatigue degradation, we need to learn more about physical solder layer looks like in healthy (new) devices and how it will change as it as it gradually degrades during operation. Modern scanning technology allows such visibility (with a significant level of detail) inside the power module's hidden layers, without destroying the device.

The following chapter presents the CT scans of three power modules focusing on the die-attach solder layers under their IGBT chips. The scans were performed

before and after power cycling of the devices at low ΔT_j amplitudes trying to mimic normal operating conditions in a converter. Due to time restrictions and other factors, the power cycling could not be completed to the desired level of R_{th} increase. However, the comparison of the scans before and after the power cycling provided a valuable insight into the structure and dynamics of the solder layer during operation, as well as a good basis for further modelling of the physical changes inside it. In terms of condition monitoring these scans allowed a better understanding of which defects lead to faster degradation, how fast is the degradation, and roughly at which stage can we expect to see any external signatures indicating its progress.

5.1 Preliminary Information

In order to be able to produce reliable future estimates of the module's solder degradation, it is important to understand the changes it experiences, as it undergoes power cycling. The best way to do this is to visually examine the internal structure of the IGBT solder layer before and after module use, for which purpose a power cycling and scanning test was devised here. A couple of non-destructive scanning options were considered, and as the solder changes before and after power cycling were expected to be very small, the one with the highest resolution was selected. The scanning equipment and software processing of the results (as specified below) were provided by the WMG (Warwick Manufacturing Group, part of the University of Warwick and based on the same campus).

Scanning Equipment:	Zeiss Xradia 520 Versa
Resolution (voxel size):	7.8 μm
Processing Software:	Scout and Scan ™ Control System
	VGStudio Max 2.2.5
	Avizo 9.0.0

It was decided to focus on the die-attach solder rather than the solder of the base plate. The die-attach experiences higher temperatures being closer to the heat source – the chip's junction – and benefits less from the temperature smoothing effects of the module's capacitance than the base plate solder, thus it was assumed that it is likely to shown signs of degradation earlier. Two scans of three modules (with 6 IGBT chips in total) were negotiated only, due limited time and equipment availability. The first scan was performed on brand new devices as unpacked and the second scan was performed after a certain amount of power cycling.

5.2 Power Cycling Regime

Some IGBT lifetime modelling studies suggest that the effect of temperature cycling with relatively small T_j variation between the hot and cold part of the cycle is not pronounced and that such cycles initially do not add to the cumulative damage experienced by the solder layers inside the module [20], [21], [62]. However, this type of power cycling with low ΔT_j represents the majority of the cycles occurring during the normal operational life of the converter and especially of the grid side inverter. Such operation of the IGBT modules is highly desirable as thus they will be undergoing lower amplitude thermal stresses meaning slower

degradation rate, but this also means that the changes in its R_{th} will less pronounced and more difficult to detect and track by a health monitoring system relying on external signals.

Because this type of operation is what the converter designers will be aiming at in real-life industrial applications, it was decided for the power cycling undertaken here to use low ΔT_j, aiming to represent the best case scenario for IGBT module solder health and longevity and the worst case scenario from the point of view of condition monitoring being able to register any changes. In fact, a risk was taken with this decision of whether the power cycling will produce any changes at all, noticeable in the scans. This is perhaps the first such power cycling and scan experiment conducted deliberately at low ΔT_j for a small number of cycles without incorporating any accelerated aging techniques. But then again, unlike most other power cycling and scanning experiments which traditionally focus on lifetime modelling and end-of-life estimation, this study is not interested in predicting when the IGBT module will fail, but simply in observing what its solder die-attach (i.e. the material layer most susceptible to creep fatigue degradation) experiences mechanically in conditions close to normal operation.

The modules selected for this study are the SKM50GB12T (opened in Figure 68).

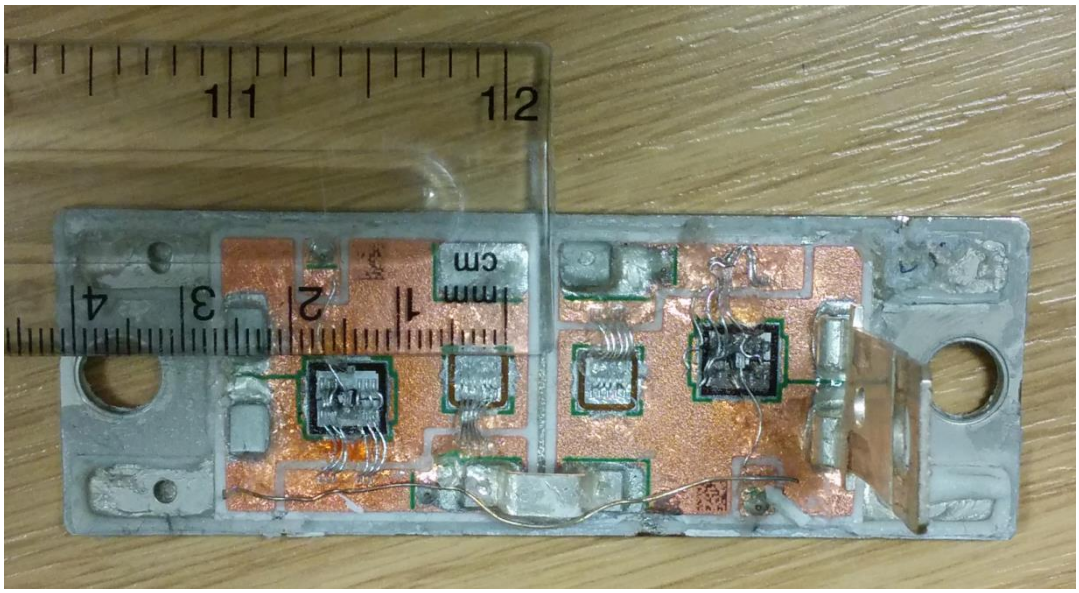


Figure 68. SKM50GB12T4 – opened module showing the DBC layout and a ruler for scale next to one pair of diode (smaller) and IGBT (larger) chips.

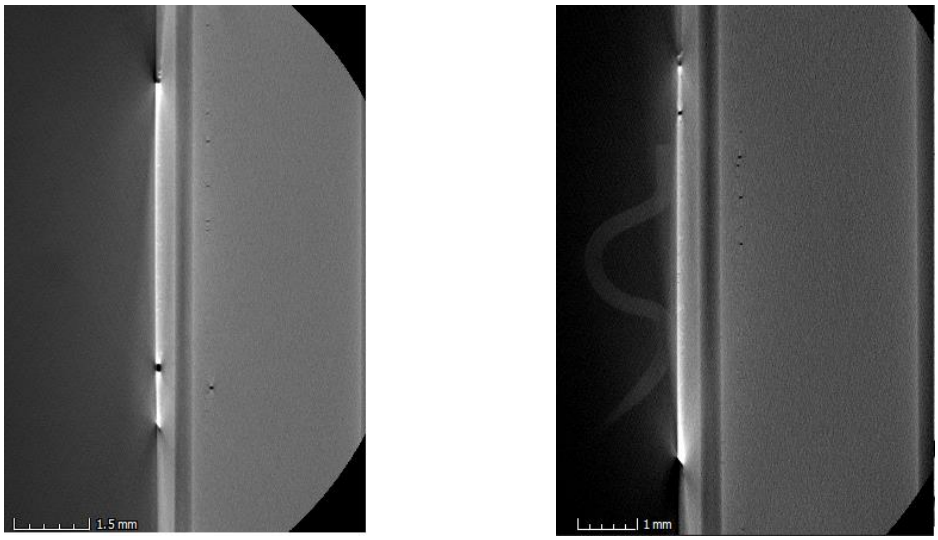
The power cycling is performed only on the IGBT chips, both conducting at the same time current step sequence supplied by a programmable current source. As the module is rated at 50A, it was decided to use current steps of 35 and 45 A for the power cycling, which with the existing cooling arrangement (water-cooled heat sink – as used in the previous experiments with Lauda WK 3200 water chiller) would provide about 17 °C step in the IGBT's ΔT_j. It was decided to use 10-second long heating and cooling cycle phases, as the aim was to have as short cycles as possible (both to avoid deep thermal cycling and because of time-restrictions). With the given quick-response cooling system, this nevertheless allowed us to achieve pronounced T_j steps up and down.

Each power module was cycled individually. This was done, so that all of them can be placed in exactly the same position on the heat sink in turn (since as it was discovered in earlier experiments that the position of the module on the heat sink had a significant impact on its measured under-case temperature, even if the modules carry the same heating current).

Within the time limitations of this power cycling and scanning experiment, each module was subjected to 35, 000 power cycles only, after which it was submitted for second scanning.

5.3 Scan Results

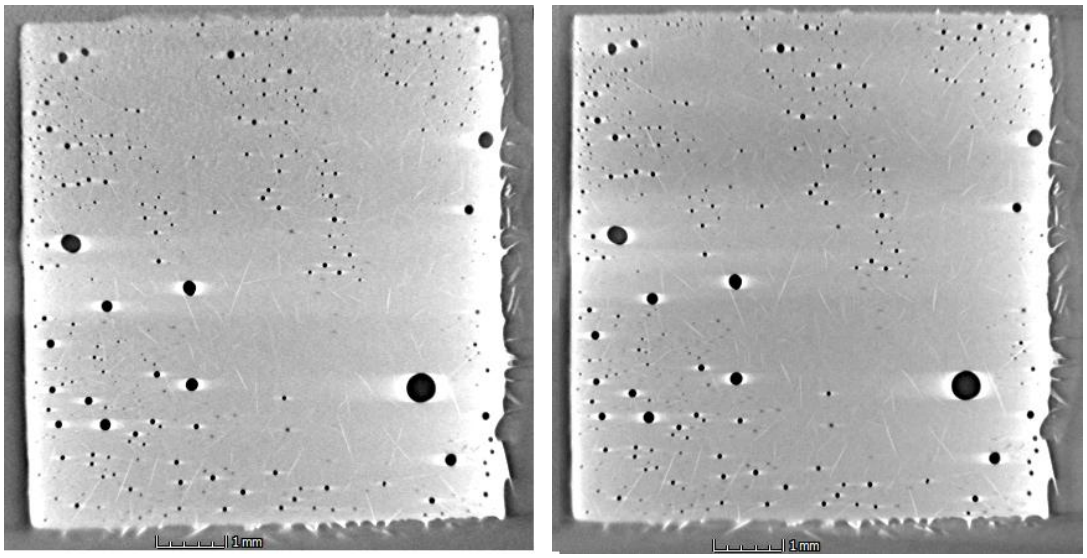
The IGBT die-attach solder scans produced 3D results which were processed and analysed by out WMG co-operators in this study. This was associated with some difficulties due to the nature of the objects scanned: with the x- and y-dimensions (length and width – about 7mm) orders of magnitude larger than the z-dimension (thickness – around 100 µm or less – meaning it could be represented by only around 10-11 voxels). Figure 69 below shows examples of side view thickness of the solder layer. It was produced in theVGStudio Max 2.2.5 software package and shows some large pores penetrating the whole die-attach solder layer. This is prior to the modules being power cycled, meaning that significant defect in the die-attach can potentially exist in brand new modules.



a b

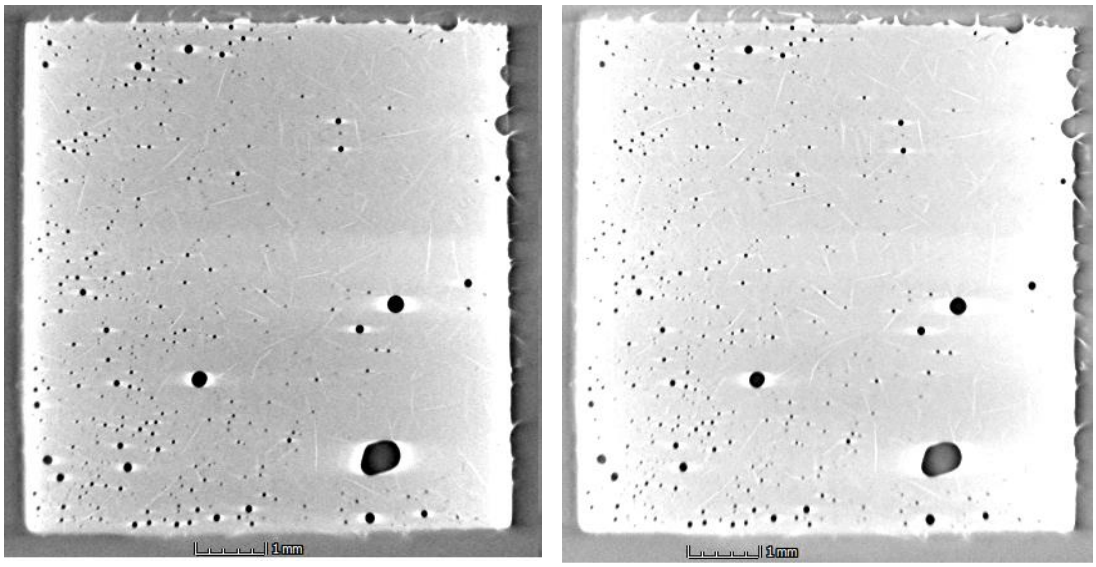
Figure 69. Side view examples – cross section of the thickness of die-attach solder: a/Module 1 – top IGBT; b/Module 2- bottom IGBT.

Despite this difference in dimensions, it was possible to process the results and provide 3D imaging and further analysis of the die-attach porosity. The photo images below represent the immediate scanning results visualised using theVGStudio Max 2.2.5 software package. They are 2D view of the 3D scans taken around mid-thickness of the die-attach layer. In each case image a/ represents the die-attach before power cycling and image b/ – after power cycling. What is immediately visible in these images is that there is significant porosity inside the solder layer to start with, as well as some gaps at edge and corner position. What is not immediately visible is the change this porosity undergoes after power cycling.



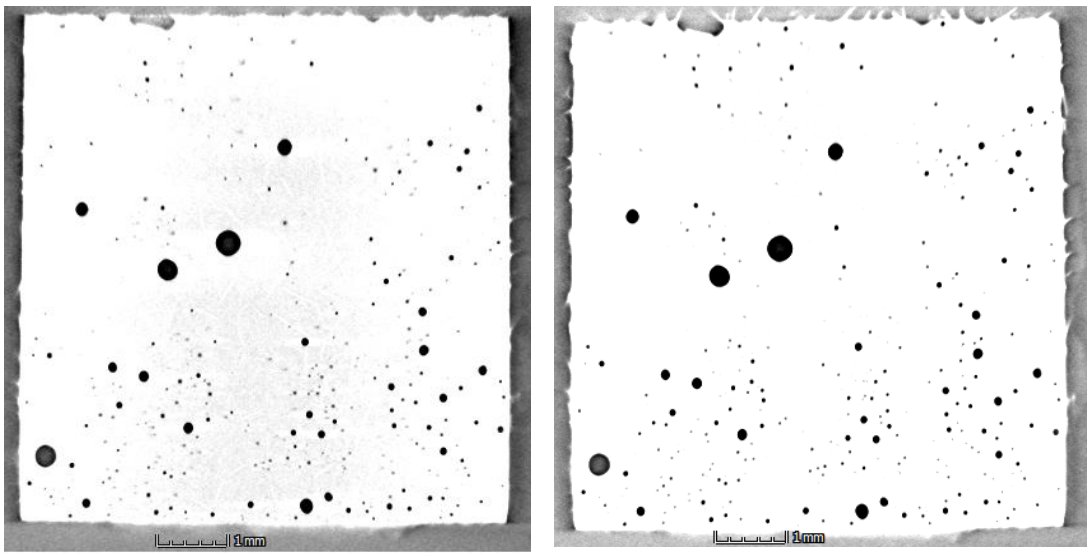
a b

Figure 70. Module 1 – top IGBT die attach a/before power cycling; b/after power cycling.



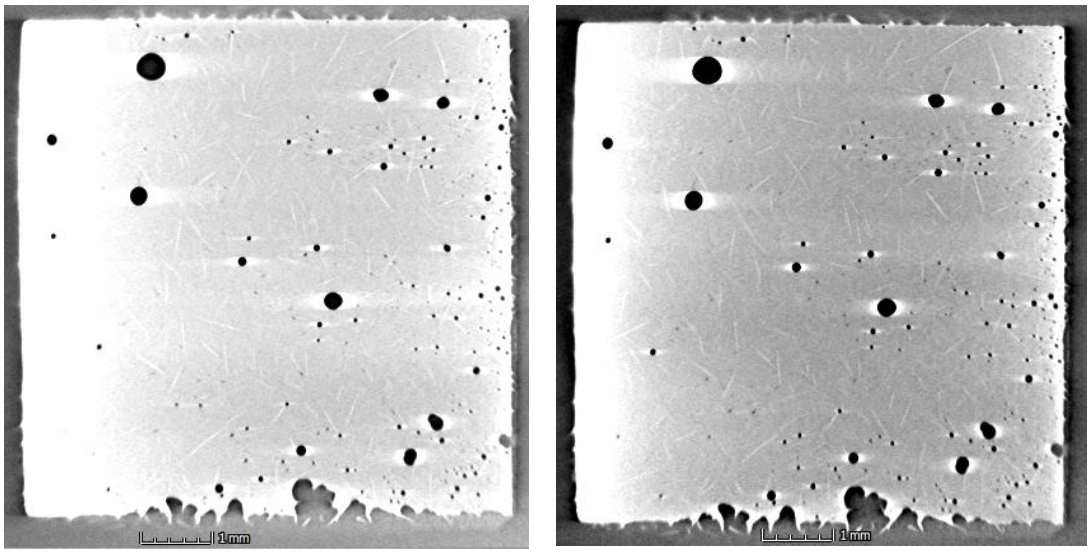
a b

Figure 71. Module 1 – bottom IGBT die attach a/before power cycling; b/after power cycling.



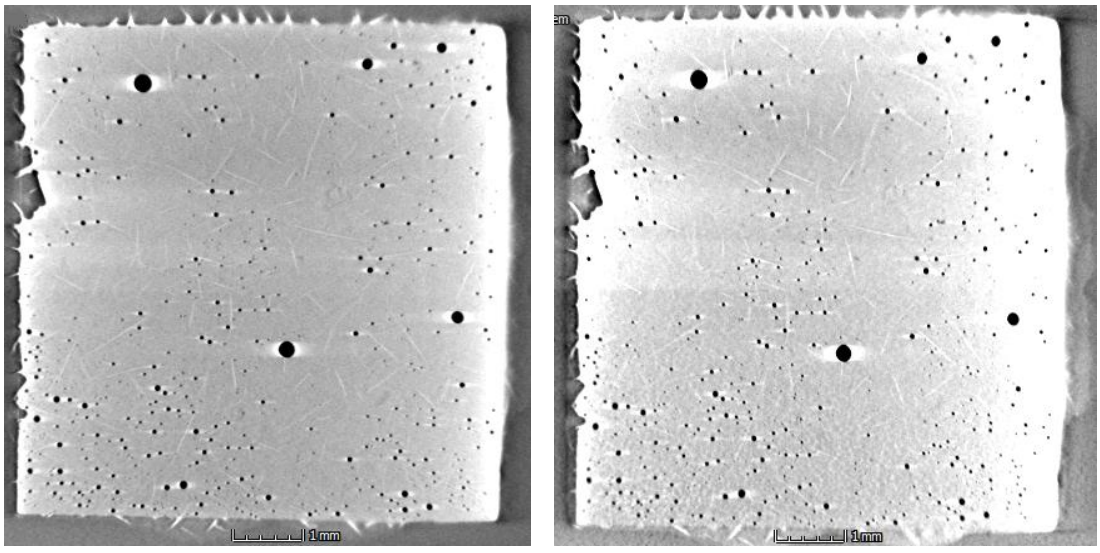
a b

Figure 72. Module 2 – top IGBT die attach a/before power cycling; b/after power cycling.



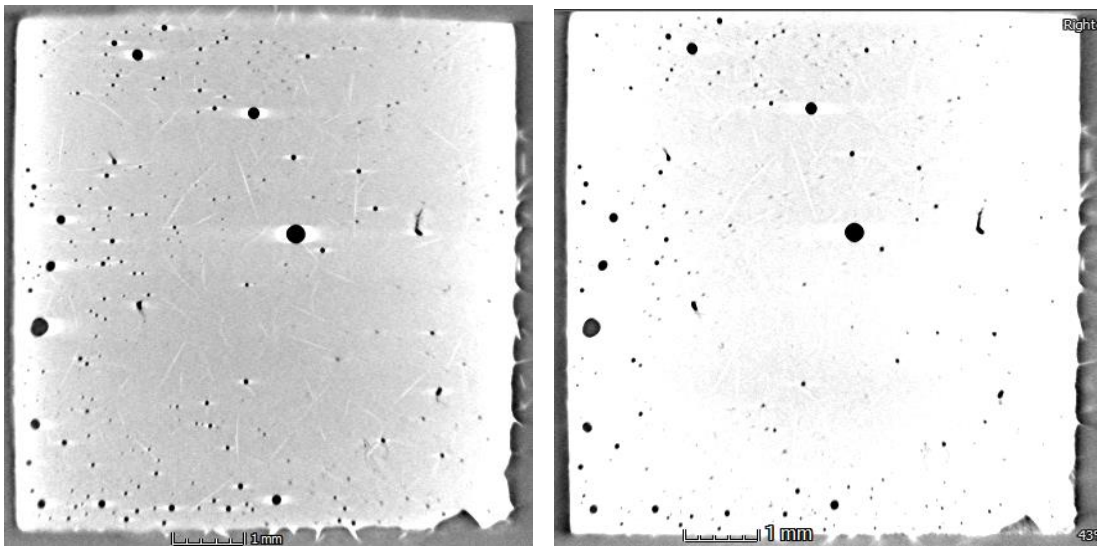
a b

Figure 73. Module 2 – bottom IGBT die attach a/before power cycling; b/after power cycling.



a b

Figure 74. Module 3 – top IGBT die attach a/before power cycling; b/after power cycling.



a b

Figure 75. Module 3 – bottom IGBT die attach a/before power cycling; b/after power cycling.

The scan images were further processed using Avizo 9.0.0, which allowed extracting numerical area and volume data of the pores. The word pore here means any void surrounded by solder material (so unfortunately the Avizo analysis excludes the edge located voids with opening outside the solder). The images below prepared in Avizo, (Figure 76, Figure 77, Figure 78, Figure 79, Figure 80 and Figure 81) present a visual comparison between the die-attach solder of each IGBT chip before power cycling and after power cycling. The pores or voids shown in them are colour-coded by volume size according to the same logarithmic scale in all images:

- Lighter blue – 0.000005 – 0.00001 mm^3

- Darker blue – 0.00001 – 0.0001 mm^3
- Red – 0.0001 – 0.001 mm^3
- Green – 0.001 – 0.01 mm^3

The minimum object size allowed by the scan is double the voxel size, but after the scan results have been cleared of noise, the smallest pore objects left are 0.000005 mm^3. Even from these 2D images, a couple of things can be observed straight away:

- The few very largest voids seem be decreasing in size in the second scan – after the power cycling;
- The middle-sized and smaller voids seem to be increasing in size and number after the power cycling;
- Generally the pores tend to preserve their shape.
- In some cases smaller pores seem to be merging into larger pores (e.g. Figure 79) and thus new pores seem to appear, while the old smaller ones are disappear (Figure 78).

The reasons for the above changes are discussed in more detail in the following section, but similar phenomena in solder layers – i.e. growth in size, merging of pores, etc. – have been previously observed to happen during the solder reflow process [104]. The principle cause of pore formation discussed there is the trapping of flux or solvent residue inside the solder layer. The pore growth is then mainly driven by the evaporation of those volatile components and the increase of pressure of the gases pushing on the sides of the pore bubble as solder is being

heated. When the gas pressure inside the pore reaches equilibrium with the opposing pressure components the pore stops growing.

In our case the heating during the power cycling of the module, although not sufficient to melt the solder, most likely resembles a succession of multiple reflow cycles at a relatively low temperatures. Heating is known to increase the diffusivity of metals and it encourages the mobility of particles within the solid material. It may allow small pores to migrate and agglomerate towards the solder interfaces in an attempt to escape.

With this is mind, the changes that have occurred in the die-attach solder layers of the power-cycled IGBT chips are not so surprising, even though the modules were subjected to a relatively small number of cycles with relatively low ΔT_j.

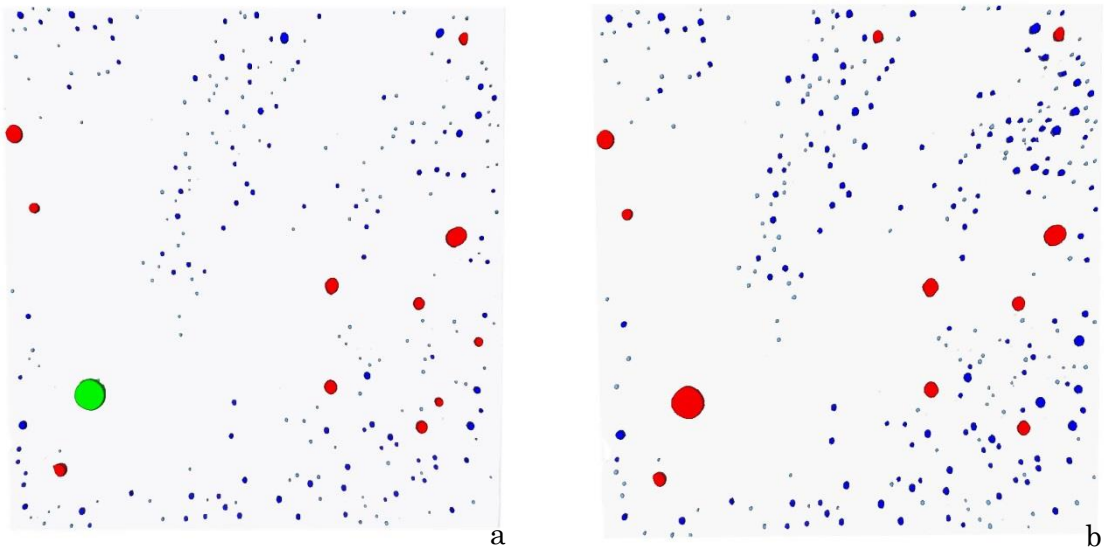


Figure 76. Scans of Module 1 – top IGBT die-attach: a/before power cycling; b/after power cycling.

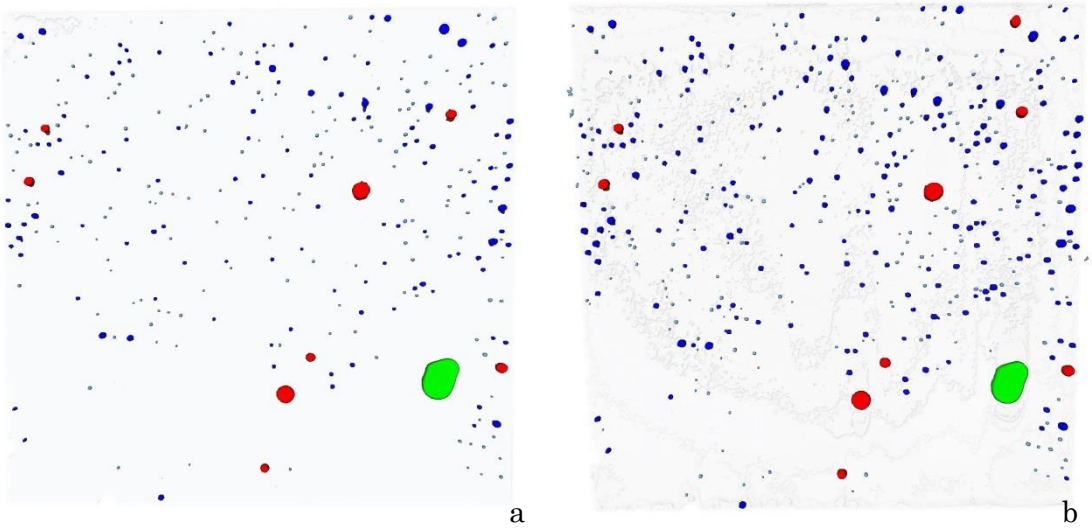


Figure 77. Scans of Module 1 – bottom IGBT die-attach: a/before power cycling; b/after power cycling.

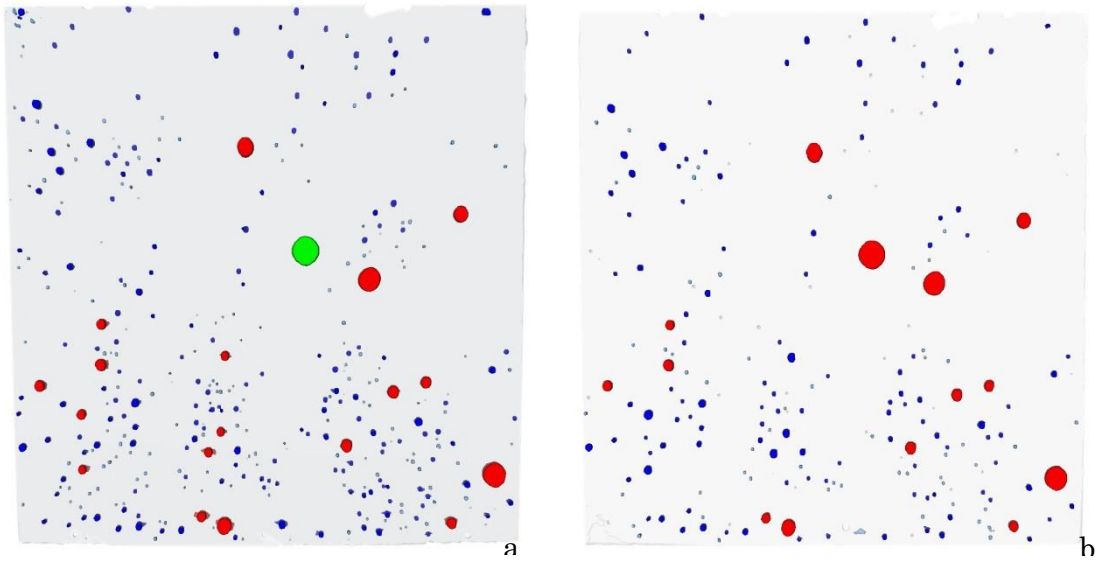


Figure 78. Scans of Module 2 – top IGBT die-attach: a/before power cycling; b/after power cycling.

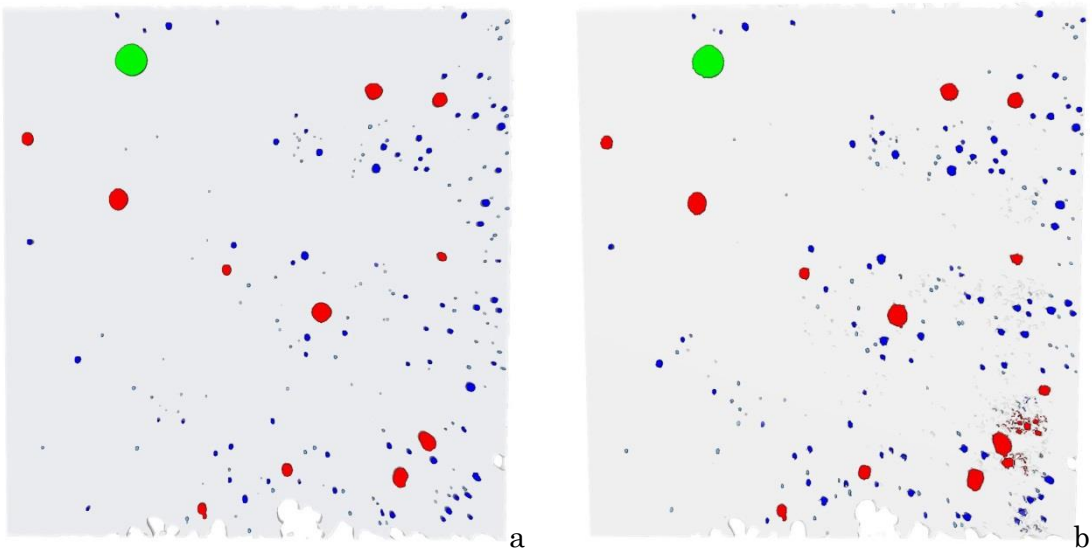


Figure 79. Scans of Module 2 – bottom IGBT die-attach: a/before power cycling; b/after power cycling.

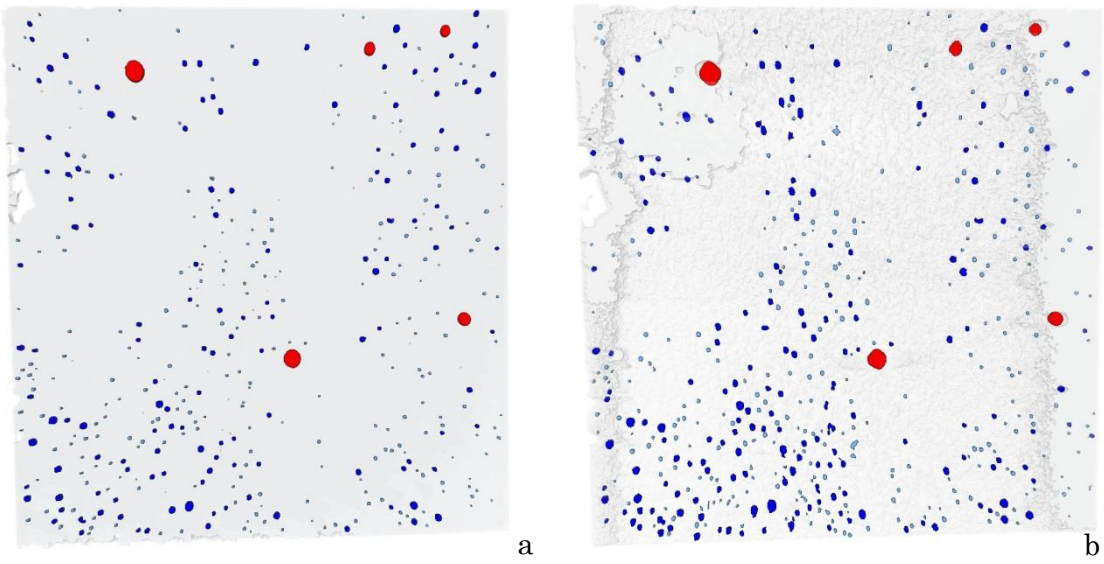


Figure 80. Scans of Module 3 – top IGBT die-attach: a/before power cycling; b/after power cycling.

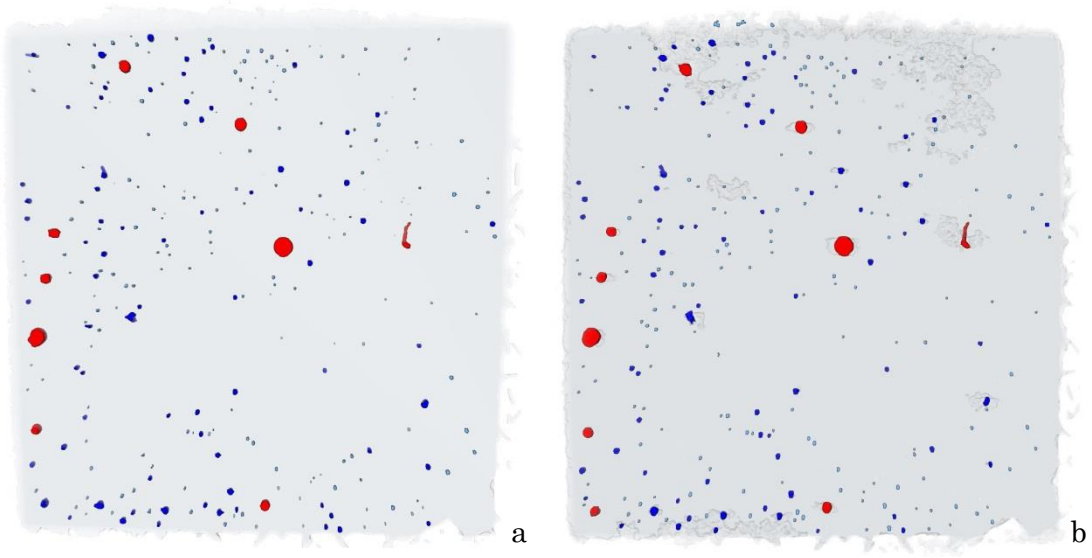


Figure 81. Scans of Module 3 – bottom IGBT die-attach: a/before power cycling; b/after power cycling.

5.4 Further Analysis of Scan Results

Apart from the above images, the post scan-software processing also provided for each die-attach scan a list of its pores with their relative xyz barycentre coordinates, their surface areas and their volumes. Initially these values were analysed by straight forward comparison of the pore sizes detected in the same die-attach substrate before power cycling (in Scan 1) and after power cycling (in Scan 2). It was found that:

- The largest pores (usually the first 10-20 largest ones out of populations with minimum 181 and maximum 482 representatives) generally have smaller sizes in the scan after power cycling;
- The rest of the pore population displays a trend of having larger sizes in the second scan for most scanned die-attach substrates. A notable exception is Module 2- top IGBT die-attach in which the pore sizes from the second scan are smaller (Figure 84). In Module 3 – bottom IGBT die attach the trend of increasing pore sizes is present only amongst the smaller pores of sizes below 0.00015 (which still represent the majority – around 200 – pore features detected by the scans) – Figure 87 .

The graphs below were shows that for majority of the pores present in the die-attach solder layers increase their volume after the power cycling. This trend is prominent amongst the smaller and medium-sized pores. (Figure 82, Figure 83, Figure 85,Figure 86)

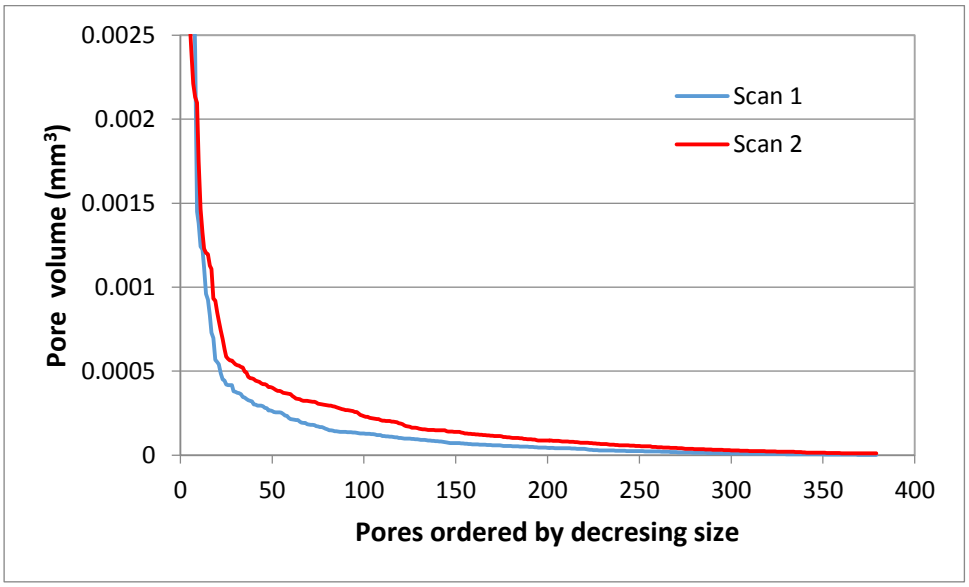


Figure 82. Module 1 – top IGBT die-attach pore sizes detected in the two scans.

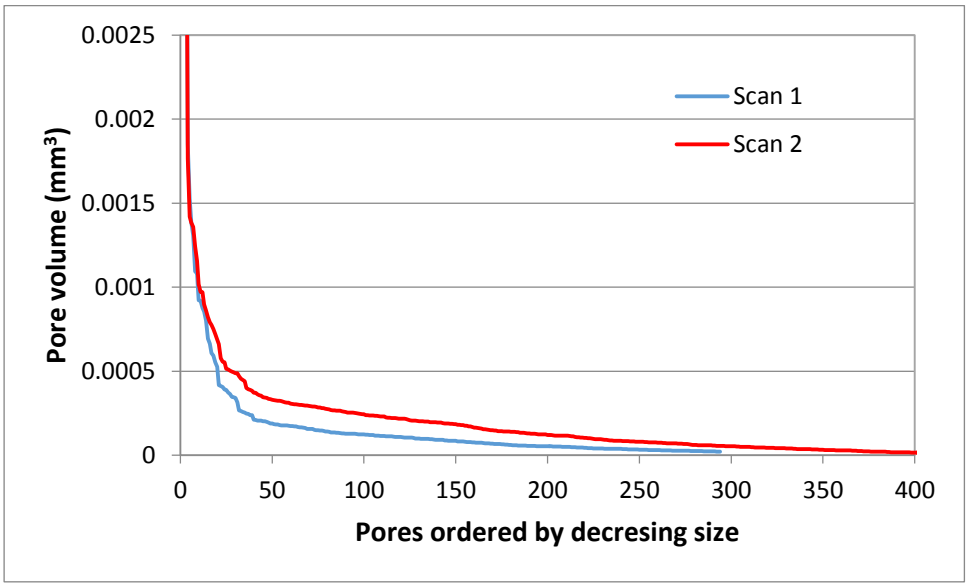


Figure 83. Module 1 – bottom IGBT die-attach pore sizes detected in the two scans.

Figure 84. Module 2 – top IGBT die-attach pore sizes detected in the two scans.

Figure 85. Module 2 –bottom IGBT die-attach pore sizes detected in the two scans.

Figure 86. Module 3 – top IGBT die-attach pore sizes detected in the two scans.

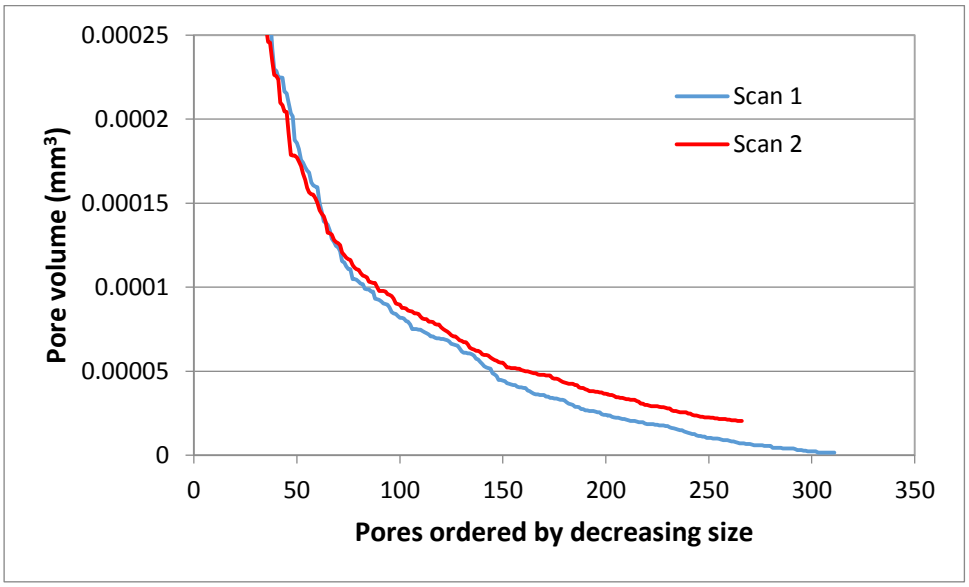


Figure 87. Module 3 – bottom IGBT die-attach pore sizes detected in the two scans.

The above comparisons refer to the pore volumes from the two scans sorted by size, but it does not necessarily compare like for like the corresponding pores in the two scans. This is obvious from the fact that we have different number of pores detected at Scan 1 and at Scan 2. So despite the fact that the above comparison suggests some pore growth must have occurred between scans, the individual pores from the first scan could have either grown, decreased in size, remained the same, migrated and merged with others or disappeared in the subsequent scan, while new pores could have become detectable. To find out which one of these happened, we must be able to determine the corresponding pairs of pores in Scan 1 and Scan 2, based on their available coordinates and size features.

Determining the corresponding pore pairs in the two scans has been problematic for the following reasons:

1. Their barycentre coordinates form the scan before and the scan after power cycling wee different. The reasons for this are complicated – a mixture of the following factors: a/the 3D scans did not include any fixed feature which can act as a reference point; b/at such fine scan resolution and with no internal absolute reference point, even very small (less than a portion of mm) difference in placing the physical module inside the scanner would have affected the the xyz coordinates of the scanned features.

2. The size, shape and thickness of the die-attach segments themselves differed slightly before and after the power cycling – most probably as a result of the power cycling and experienced thermal stresses. As Table 9 suggests, the die-

attach substrates appear to thin-out (often by considerable amount – around 30 µm) while spreading out slightly to the sides. The dimensions in the table were obtained from the largest relative distance between detected features along each axis of the 3D coordinate system – x (length), y (width) and z (thickness).

Table 9. Change of die-attach dimensions between Scan 1 and Scan 2.

	X - Scan1	X - Scan2	Y - Scan1	Y - Scan2	Z - Scan1	Z - Scan2
M1-T	7.2999	7.40299	6.722769	6.711387	0.108253	0.071989
M1-B	7.25633	7.63589	6.775437	6.989706	0.096971	0.072757
M2-T	7.15421	7.15542	6.749193	6.74818	0.080328	0.053478
M2-B	7.09448	7.0863	6.43316	6.42025	0.068982	0.060083
M3-T	7.18759	7.27068	6.729386	6.749636	0.061321	0.05583
M3-B	7.21085	7.46365	6.717312	6.68447	0.093473	0.063759

3. The detected pore numbers were different in the before and after scans:

a. In some cases after the power cycling new pores seem to have "appeared" in the second scan. This can be explained with the presence of very small pores – undetectable in the first scan – which have grown (e.g. by merging together with other minute pores) during the power cycling to become visible in the second scan.

b. In other cases after the power cycling some old pores seem to have "disappeared" in the second scan. This can be explained with pore migration (which can happen if the solder layer stretches as pointed in 2.) Another way pores can be "lost" from the original count is through merging with other pores. Also, pores located very close to the edges or interfaces of the solder layer can be cleared off as

noise or not counted as pores, if they are fully surrounded by solder material. Unfortunately the processing software Avizo (which produced the lists of pores from the scans) is not capable of capturing the dimensions of such open voids, and thus they are excluded from its porosity analysis.

4. Even when the same pores are present in both scans, if one scan registers a change in their size, their barycentre coordinates can migrate.

5. Differences in pore coordinates from the different scans may also be affected to a certain extent by removing measurement noise, although its effect should be small in proportion.

In spite of the above difficulties, the sorting of corresponding pores from the two scans was still attempted by using an approximate matching algorithm implemented in MATLAB. The idea behind this algorithm is to take the combined information we have available about a given pore (i.e. its three xyz coordinates, its volume and its 3D surface area) as pore-defining matrix and then to look for the closest approximate match of each such matrix from the Scan 1 list to another in the Scan 2 list. This matching does have its limitations. It will not be able to capture correctly the fact that several pores may merge into one, as it will use the closest match of only one of the smaller pores to the resulting big pore. It may be confused by the presence of a lot of small pores close together or by the fact that the thinning and spreading out of the solder layer may have moved pore into the original coordinates of another pore of similar size – thus while visually a pore from the can be identified to its correct later self in the second scan, the algorithm

may accidentally match it to different pore. Also it should in effect separate the non-matches (pores which have either appeared or disappeared), but if the number of pores in both scans is very close and the sizes and coordinates of pores are very similar, it may try to match a newly appeared pore, for example, while discarding the one corresponding in reality.

Having said that, this approximate matching provided the best sorting option, outside having each individual pore pair visually matched by a human analyser (which given further time and resources to research this topic can be suggested as future work). Most of the pores (at least the ones shown in the scan images) have not migrated dramatically in relation to each other or changed significantly otherwise and the number of pores that have appeared or disappeared is not large relative to the number of pores present in both scans. Thus the occurrence of possible incorrect matches produced by the algorithm should be sufficiently low for our purposes.

After implementing the matching of corresponding pores, the comparison of Scan 1 and Scan 2 confirmed that:

- The small number of very large pores experience decrease of size in Scan 2 – i.e. after the power cycling. These are pores that penetrate the solder layer assuming instead of a globular shape, a shape closer to a cylinder and their decrease in size is explained with the fact that when the solder layer thins out (as found from Scan 2), they lose height while maintaining roughly the same circumference. Some COMSOL modelling results presented in the next section

confirm that as a void grows larger its growth rate slows down. They also suggest that at the circumference of the interface where such voids connect or attach to the next material layer, cracks can start growing as a result of the sheer stresses from thermal cycling of materials with different CTEs. The term crack is used here to denote horizontally spreading thin void initialising the delamination, separation or peeling off of the different material layers. As such features at their initialisation stage are very thin (of thickness much less than 10 μm as suggested by the COMSOL simulations) they will be undetectable by the resolution of the scans described here. In effect the largest pores in our samples may have lost some of their volume to the formation of a newly initialised crack at the interfaces with the other material layers, but unfortunately this is impossible to confirm by the scans performed here, or in the given circumstances, by any non-destructive scanning means.

- The other trend confirmed by the matching pores analysis is that the majority of medium and smaller size pores tend to increase in size. Unlike the previous more statistical approach, however, after the pore matching it can be seen that individual smaller pores can be decreasing in size as well and that pores of very close starting size may have undergone may be undergoing changes at different rate as some would have increased proportionally more than the others. This is something to be expected. As mentioned earlier one of the main mechanism of void growth which can be used to explain why we see pore size increase in our samples given the very short duration of power cycling and the relatively low

thermal amplitudes, is the merging, or absorption of smaller pores into a bigger one. Depending on the starting pore size and numbers, it is not surprising to get pores displaying different amount of change in their volume. The graphs below illustrate the comparison between the volumes from the first and second scan of corresponding smaller sized pores (as matched by the approximate matching algorithm).

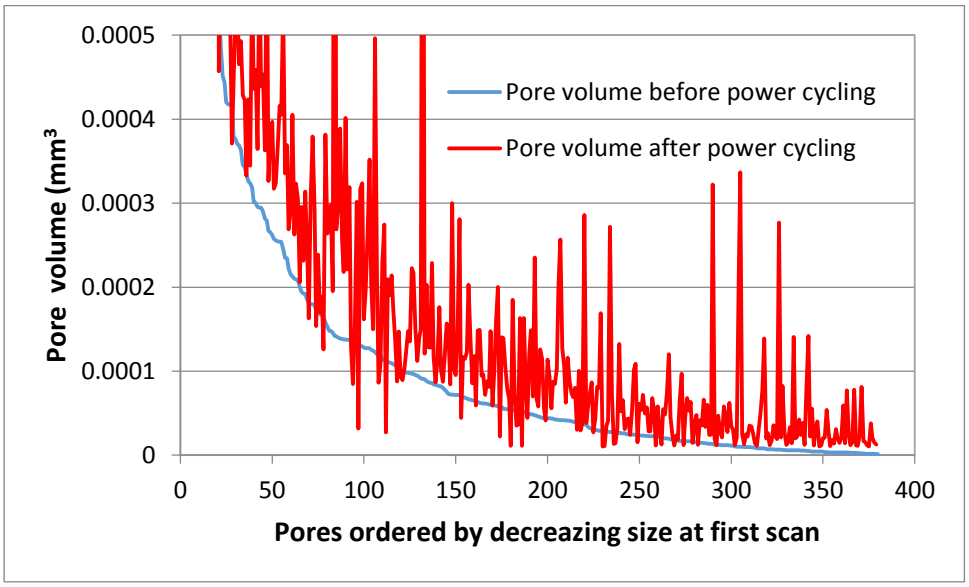


Figure 88. Module 1 – top IGBT die-attach: pore volume change before and after power cycling (large pores are excluded from this plot).

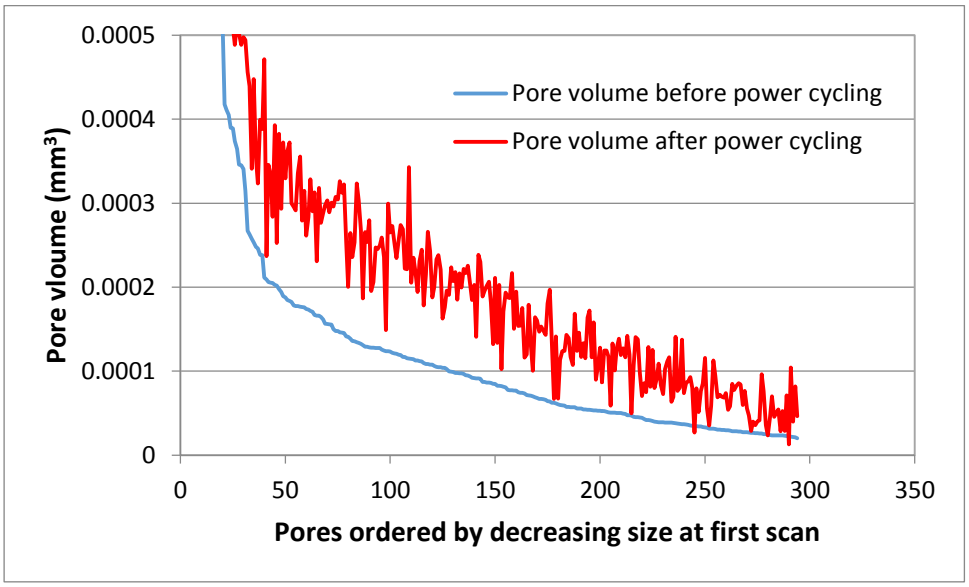


Figure 89. Module 1, bottom IGBT die-attach: pore volume change before and after power cycling (large pores are excluded from this plot).

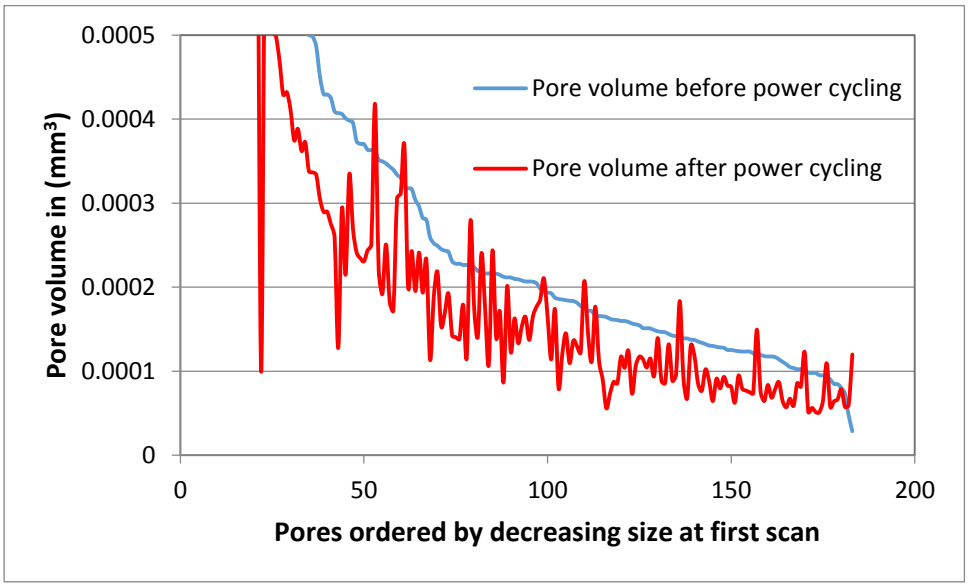


Figure 90. Module 2 –top IGBT die-attach: pore volume before and after power cycling (very large pores are excluded from this plot).

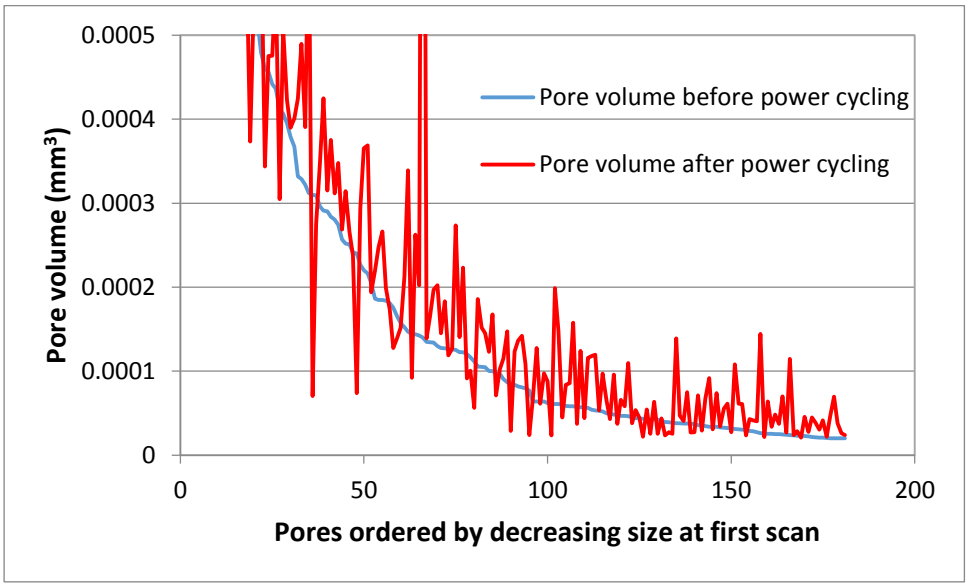


Figure 91. Module 2 –bottom IGBT die-attach: pore volume before and after power cycling (very large pores are excluded from this plot).

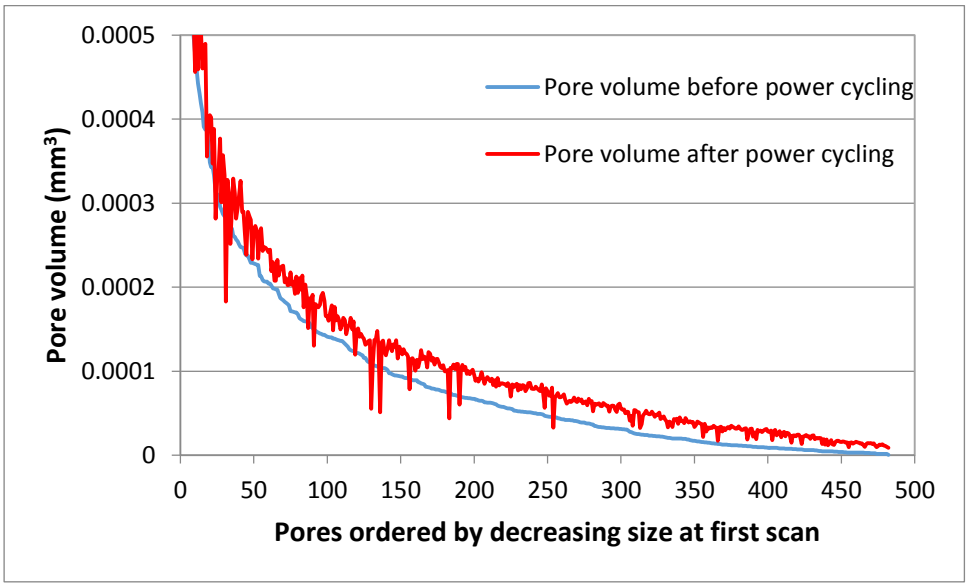


Figure 92. Module 3 – top IGBT die-attach: pore volume before and after power cycling (very large pores are excluded from this plot).

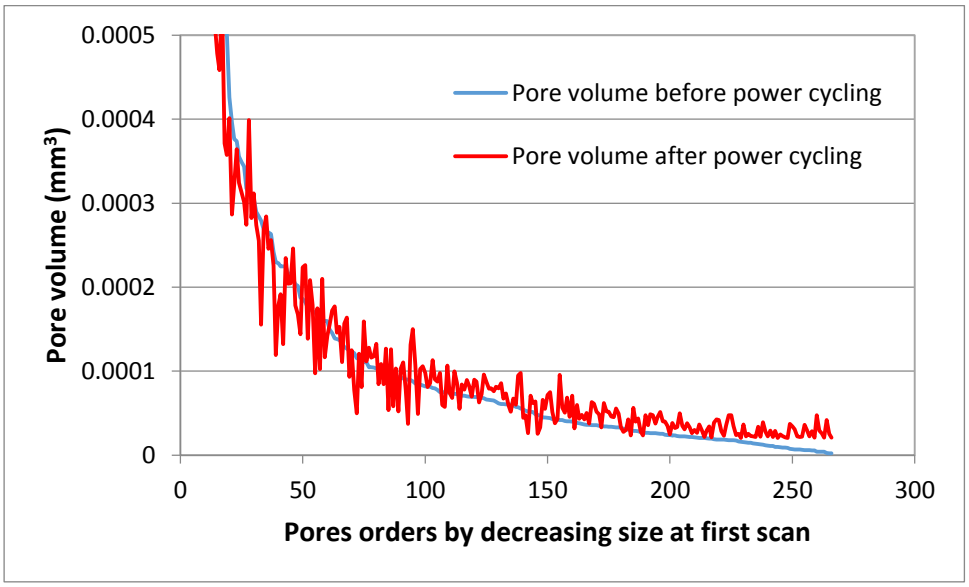


Figure 93. Module 3 – bottom IGBT die-attach: pore volume before and after power cycling (very large pores are excluded from this plot).

Again the scans of Module 2- top IGBT die-attach show that its pores are decreasing in size. This can be explained with pore positioning close to the top and bottom surfaces of the scanned die-attached layer and their thinning as the layer itself thins between scans (from around 80 to around 53 μm). Following this the pore size cuts can also come as a result from the shaving-off of the noise at the die-attach solder layer interfaces. Another example of more significant thinning (of about 30 μm) is observed also in Module 3 – bottom IGBT die attach, which like Module 2 – top IGBT die-attach shows larger number of pores that decrease in size than are present in the other samples which have not lost as much thickness.

In conclusion of this part of our porosity scans analysis we can say that:

- Porosity seems to be a common feature of the die-attach (and base plate) solder layer – resulting from the manufacturing process. Not many FEA models of IGBT module solder account for the large number of pores of different sizes present from the very start of the operational life of the device.

- Most IGBT module lifetime models predict minimum several years of module operation before degradation becomes noticeable and most similar scans done so far are of modules with higher degree of wear-out. In this light, the changes observed in the scans described above are surprising after such short period of shallow power cycling, but their presence is undeniable. These scan result can further inform and changed the current methods for IGBT module lifetime modelling and FEA modelling of the voids and cracks in the die-attach solder layer.

- The scans show that a lot of the pores have grown after the power cycling and some new pores also appear occasionally. How does this happen? The pores are essentially bubbles of trapped gas (as it is impossible for vacuum to create a void within a solid or liquid and even less do so in a globular shape fashion). It is true that the junction temperatures which the devices were estimated to reach during the power cycling were not high enough to melt the solder, but the growth of pores still suggests that a process of gas expansion, permeation and recombination with other trapped bubbles through the solder layer is possible. And that this is likely being facilitated as the solder is heated by the power cycling and with the aid of the stresses resulting from the different rates of thermal expansion and contraction of

materials with non-matching CTEs. Such merging and emergence of pores can be visually observed in Figure 79.

- The above bullet point also explains the fact that the scans before and after power cycling show different number of pores (with a difference in number as small as 1 in the scans before and after of Module 1 – top IGBT die-attach and as large as 191 after of Module 3 – top IGBT die-attach.) This difference in numbers has made matching of corresponding pores in the two different scan difficult and the interpretation of the scan results more complicated. This work may benefit of revisiting the pore matching process using visual matching by human analyst.

- Another important finding which bears reference to the reasons why in some of the scanned samples we observe more pronounced decrease in pore size is the fact that after the power cycling the solder layer appears thinner in the second scan. This spreading effect is not taken into account by a most FEA models, yet it appears to be physically present.

- We would like to acknowledge the fact that our observations are made on the basis of six die-attach scans only. This type of work would benefit from further scanning and examining more samples. However, the scanning process is expensive and time consuming (over 12 hours for Individual die-attach scan only and weeks to process the results into a form in which they can be compared and further analysed) and thus not is has been easy to obtain a larger sample base.

5.5 Discussion and Further Modelling

The scans show clearly that some internal porosity exists within the die-attach solder layer from the device's start of life and that changes in this initial porosity can be activated even by relatively small number of power cycles well within the device's rated current and with relatively low ΔT_j variation. However, both lifetime models of power modules and experience from their industrial use indicate that the modules do not display external signs of aging or performance deterioration for years of operation. This means that the existence, growth and migration of small pores must not be affecting significantly the R_{th}, and therefore also the power loss of the module – i.e. the heat flow path must not be compromised by a pore, if it can easily go around it. The question is: when the does the growth/mobility of the pores become a problem?

Some COMSOL modelling work was carried out following on from the 3D X-ray scan findings. It suggests that the pores distributed within the solder die-attach layer tend to grow towards the solder chip interface and to form crack R_{th} increasing –i.e. horizontally spreading features growing along the x and y axes and leading to progressive delamination or peeling off of the chip from its substrate.

A 2D symmetrical finite element model of the SMK50GB12T4 IGBT die-attach was developed to evaluate the thermomechanical behavior of a solder layer with initial defects and to investigate the crack development and growth process (Figure 94). It allows the estimation of fatigue damage by indicators such as the

von Mises stress, the creep strain, plastic strain, creep energy density and inelastic energy density.

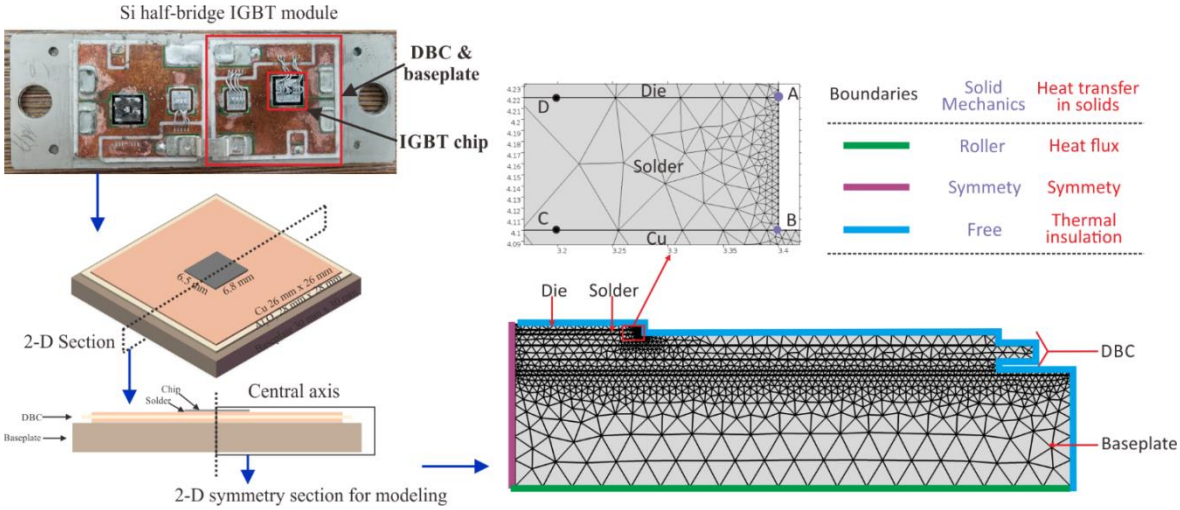


Figure 94. FEA model prepared in COMSOL for the SKM50GB12T4 (1200V/ 50A) module transferred to a 2D symmetry representation.

The boundary conditions in the COMSOL model aim to represent the power cycling conditions between Scan 1 and Scan 2, (ΔT_j 17.5˚C, T_m 68 ˚C). The model investigates the behaviour of two types of defects within the solder layer – cracks (or horizontally spreading defect) and pores (or void of more or less globular shape). Initially, it shows where the highest stress distribution is within the solder layer profile, assuming no initial defects (i.e. at the outer corner of the chip and solder interface as shown in Figure 95). This also is where the any initial defects, if present, should experience the fastest growth rate. The model shows that the

stresses along sharper edges such as observed in crack are higher and the general direction of defect growth is from edge to centre.

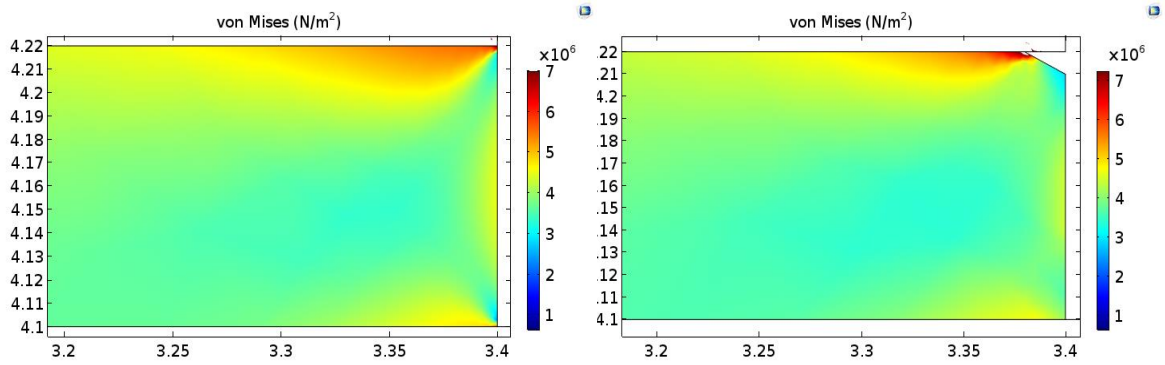


Figure 95. Stress fatigue distribution within the solder layer without initial defects and with a crack inserted in the area subject to the highest stresses.

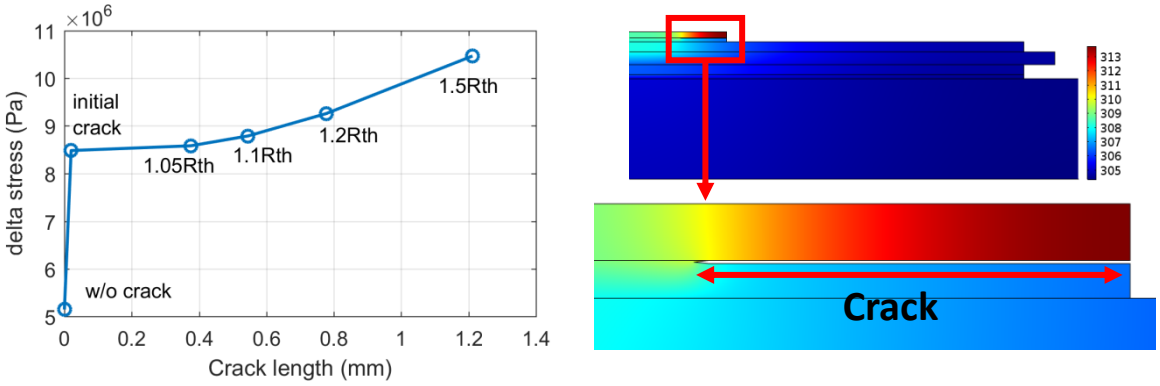


Figure 96. Relationship between stress fatigue, crack length and R_{th}.

The thermal resistance will increase with the length of a crack (Figure 96). In this vertical cross-section 2D model this length corresponds to the crack surface as viewed in the horizontal plane of a 3D model. Its increase logically leads to

increased junction temperature which will further enhance the stress concentration along the chip-solder interface and facilitate delamination.

According to the COMSOL model for a crack to develop without any initial defects, it can take many decades. However, the X-ray scans clearly indicate that this is not the case – real-life die-attach solder layers include hundreds of pores and most likely also defects at the edges of the solder layer and along its interfaces with the chip and the DBC. Therefore modelling solder layer with at least one initial defect provides closer representation of real-life solder layer degradation-rate.

Simulations of the presence of individual voids of varying radius was out and it was discovered that the stress concentration in the case of a round void inside the die-attach layer is highest at its top and bottom edges(slightly higher at the top), causing the void to deform vertically in these directions by accumulating fatigue damage.

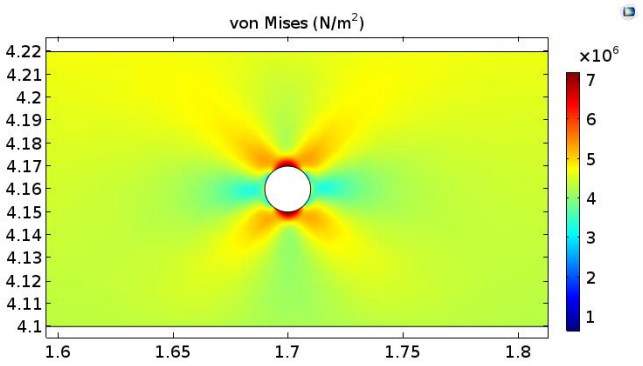


Figure 97. Stress distribution on solder layer with 10 µm void.

Simulations with different pore radii confirm the observation from the scan results that voids of smaller radius are likely to have faster growth as a larger radius of curvature reduces the stress density concentration and slows the void growth rate (however for very small pores the deformation space is also smaller, voids of around 10 µm radius are shown by the model to grow at fastest rate – as presented in Figure 98).

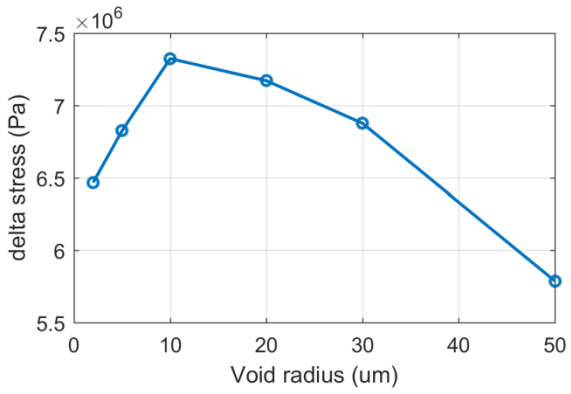


Figure 98. Stress fatigue on the edges of voids of different sizes.

When a large void reaches the chip-solder interface, the highest stress concentration it experiences according to the COMSOL model will be in its left corner (Figure 99). The local stress there is much higher than the highest stress level experienced in the corner of solder layer without a defect and this will initiate at this position a crack between the two materials as they expand and contract at different rates during power cycling.

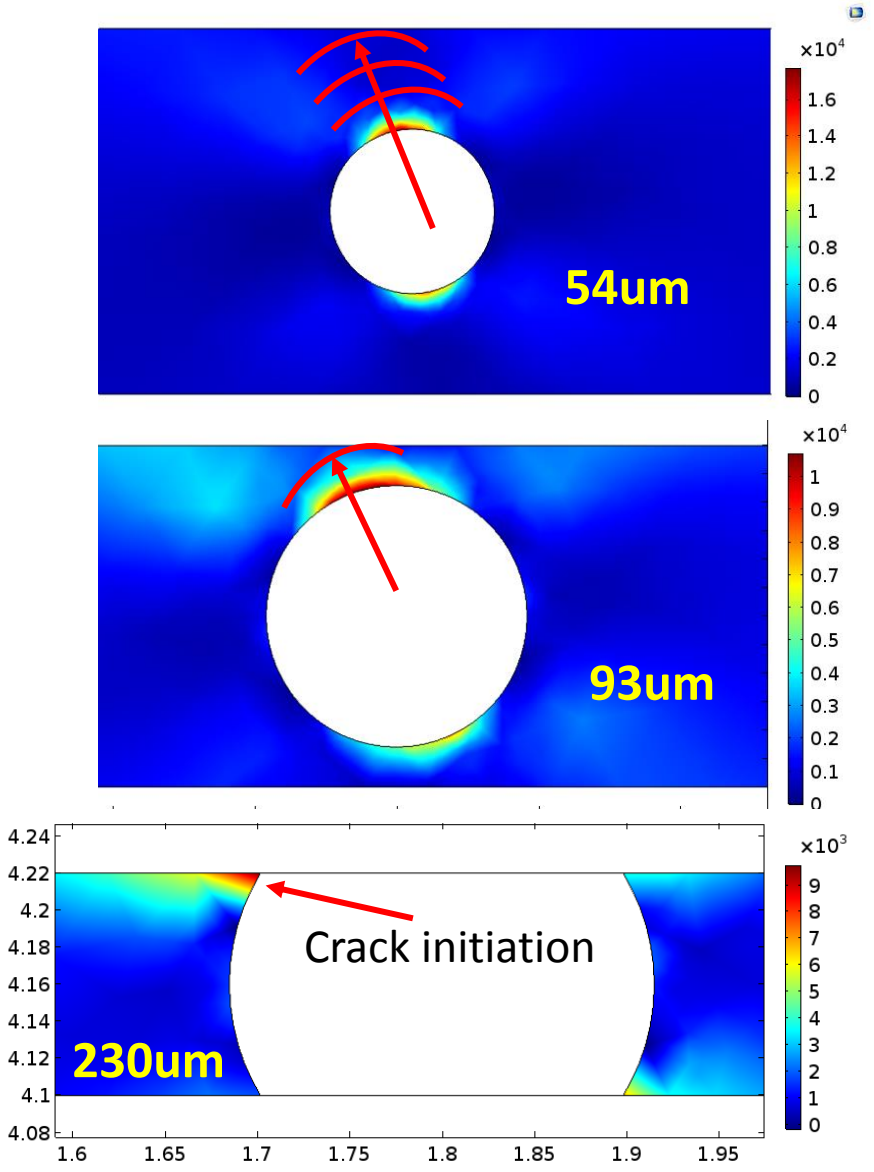


Figure 99. Growth process of a pore within solder and the creep energy density distribution around it (simulations with T_{jm}=60°C, ΔT_j=30. Resulting crack growth rate for 0.23mm diameter void is 0.22 um/cycle x10^3 (2 µm/day) which will take only 2.97x10^6 cycles (343 days) to increase of R_{th} to1.2 the original value).

Overall the COMSOL model suggest that for a single smaller pore to grow, reach the reach the chip-solder interface and begin to develop cracks along its corners touching the interface, it would take a long time (around 40 years). This is why the impact of small voids may not be immediately observable in terms of R_{th} increase. However, as their number in the scanned samples is high, this single pore growth model may not be exactly representative of the time scale necessary for them to show externally impacts on the R_{th}. The impact of a single crack takes shorter time to manifest in terms of increased R_{th} based on the model (around 10 years). The findings of the model are in line with (and contribute to) the observations from the scan, however, modelling of multiple defects is suggested as further work which can provide a better representation of the actual changes in the solder layer during power cycling.

5.6 Conclusions

The conclusions from this chapter focusing on the internal structure and the thermomechanical changes brought about by power cycling within the solder die-attach layers of IGBT modules are as follows:

- Significant level initial solder porosity is observed even in brand new modules.
- Some of the pores have sufficiently large dimensions to span the entire thickness of the solder layer.

- Following power cycling with low number of cycles moderate mean T_j and low ΔT_j there are changes in the porosity observable from the scans.
- The solder layer thickness appears reduced in the post power cycling scan, pointing to lateral spread.
- The smaller pores display a trend of increase in volume, while the larger pores show decrease (the decrease is explained with pores preserving their top-view circumference, but losing height due to layer thinning).
- The number of pores also changes as new pores appear in the post-power cycling scan or pores disappear (explained with merging into new pores) and the location coordinates of the pores also change slightly.
- Regardless of these obvious changes the modules do not show external significant signs of solder degradation.
- FEA modelling using COMSOL indicates that this is due to the fact that:
  - Crack (delamination type defects) rather than globular voids are the main reason for R_{th} increase.
  - The growth of a globular void inside the solder layer becomes progressively slower as it grows in size as the larger curvature will gradually lead to a reduced stress concentration along its border, (whereas the growth of cracks becomes progressively faster and the stress concentration on their leading edge intensifies). Before the voids touch the chip-solder and solder-DBC interfaces they do not obstruct significantly the heat flow path from junction to case (which goes around them).

- Once a void reaches the chip-solder interface, it will experience higher stresses concentrated on its corners of contact, from where cracks will start growing – at this stage the void will begin to influence the module's junction to case R_{th} more significantly.

For the further work, it is suggested that it would be beneficial to evaluate the combined impact of the several voids within the die-attach with example distances and positioning configurations that can be obtained from the scan. This will show how the voids would interact and how much their interaction would affect the module's reliability. It is also recommended to continue power cycling and do another round of scans on the three X-rayed modules aimed mores specifically at detecting a crack formation especially at the edges of large pores penetrating the solder die-attach layer and "touching" the chip interface. This work would further have benefited by additional scans of the same modules after being cycled to within close to 20% R_{th} increase and to perhaps to 50% increase.

In terms of our focus on condition monitoring, this delving into the die-attach solder material dynamics has revealed that:

- Voids usually do not do not cause increase of the R_{th} and thus cannot be detected by external temperature measurements;
- However, if they merge into larger voids adjoining the chip-solder interface and spread laterally into cracks their influence will be felt proportional to the surface area they cover – such defect may be detectable by condition monitoring.

Chapter

6 Practical Health Monitoring Method

This chapter focuses on the development of temperature based IGBT module health monitoring concept and algorithm. First it presents the experimental work with heat and heat sinks undertaken with the aim to develop a better understanding of the thermal phenomena that can be affecting the devices in operation and the externally obtainable signatures of their healthy or deteriorated performance. It then follows on with defining what is necessary for temperature based health monitoring of IGBT modules in wind turbine converter applications and presents further experimental work related more specifically to the suggested condition monitoring concept.

6.1 Initial Thermal Experiments

This section presents in brief the initial heat experiments conducted to develop first-hand understanding of how solder degradation affects the IGBT's

electrical performance and the impact of junction temperature on the IGBT's electrical performance (i.e. the changes of its current and voltage signals with increase of T_j).

6.1.1 Pulse test on healthy and degraded modules

Experiment goal

The goal of this experiment is to find out whether there is a difference in the electrical signals of degraded and non-degraded power modules measured for a single switching pulse at the same junction temperature (T_J) achieved in a thermal chamber.

Equipment list

- Inductive Switching Rig with Thermal Chamber at the School of Engineering, Warwick University – the rig includes pulse control and measurement equipment.

- Devices under test (DUT): Semikron half-bridge modules SKM50GB12T4 — degraded and non-degraded

Experiment description

The DUT (device under test) is placed in the thermal chamber set to a given temperature level. Voltage and current are supplied to it from the rig using a pre-configured 2-pulse sequence (pulse allowing the charging up of the inductors

(250us) and one short pulse (20us) for performing the measurements on the DUT). Measurements are performed and saved using a Techtronics oscilloscope.

Experiment results and discussion

The experiment result: At the same junction temperature there is no significant difference in the electrical (current and voltage) signals of the new and degraded modules—as can be seen in Figure 100, Figure 101, Figure 102 and Figure 103 below. The notation: New, Old-0, Old-1, etc. refers to new un-used module without degradation, Degraded module 1, Degraded module 2, etc.

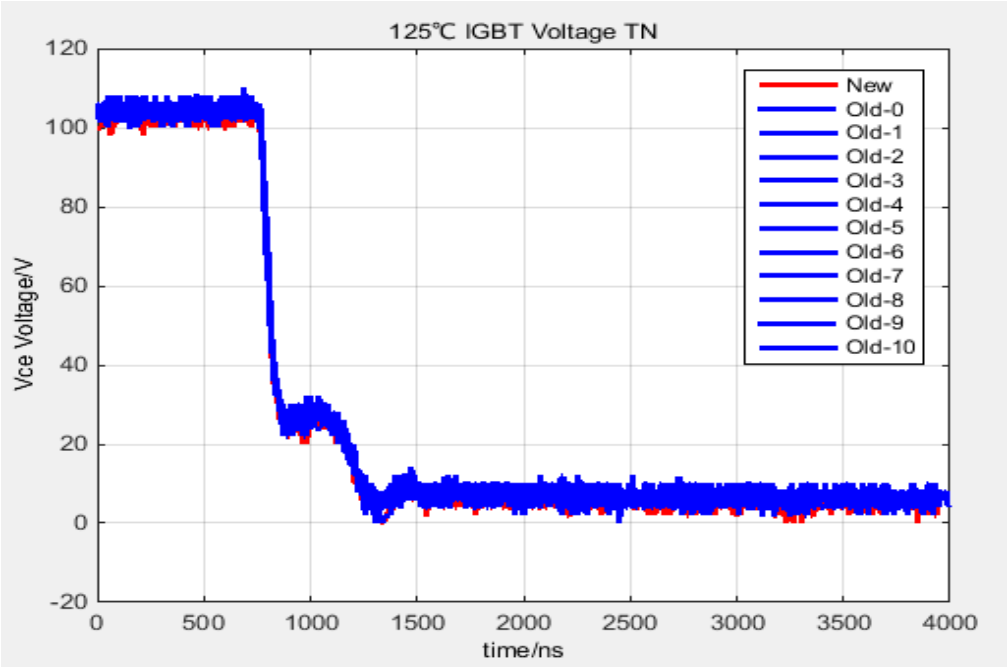


Figure 100. Inductive switching test results at 125 °C: turn ON IGBT Voltage curves

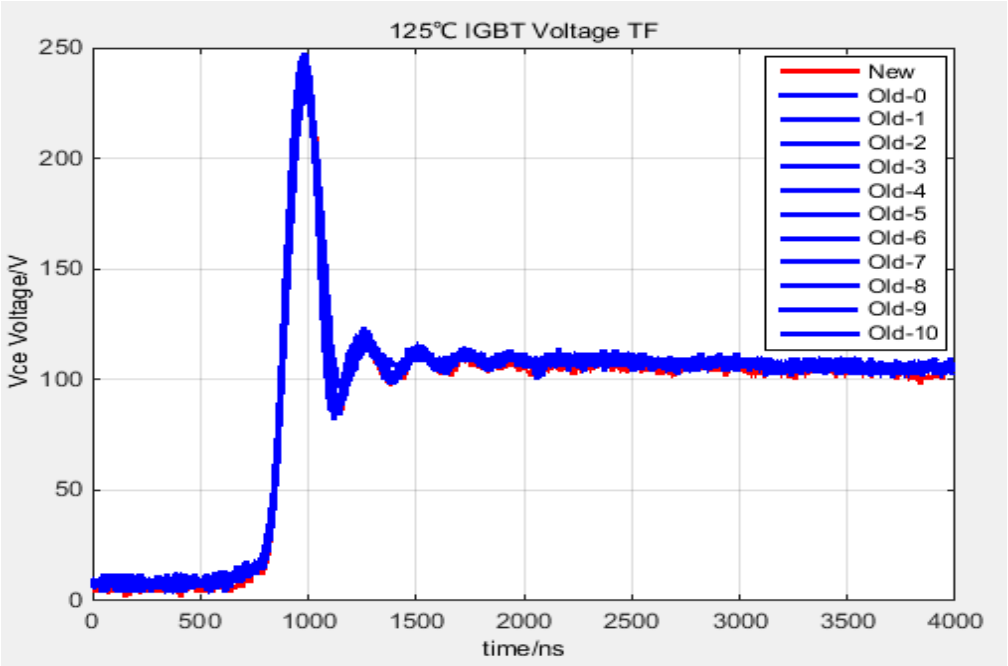


Figure 101. Inductive switching test results at 125 ℃: turn OFF IGBT Voltage curves.

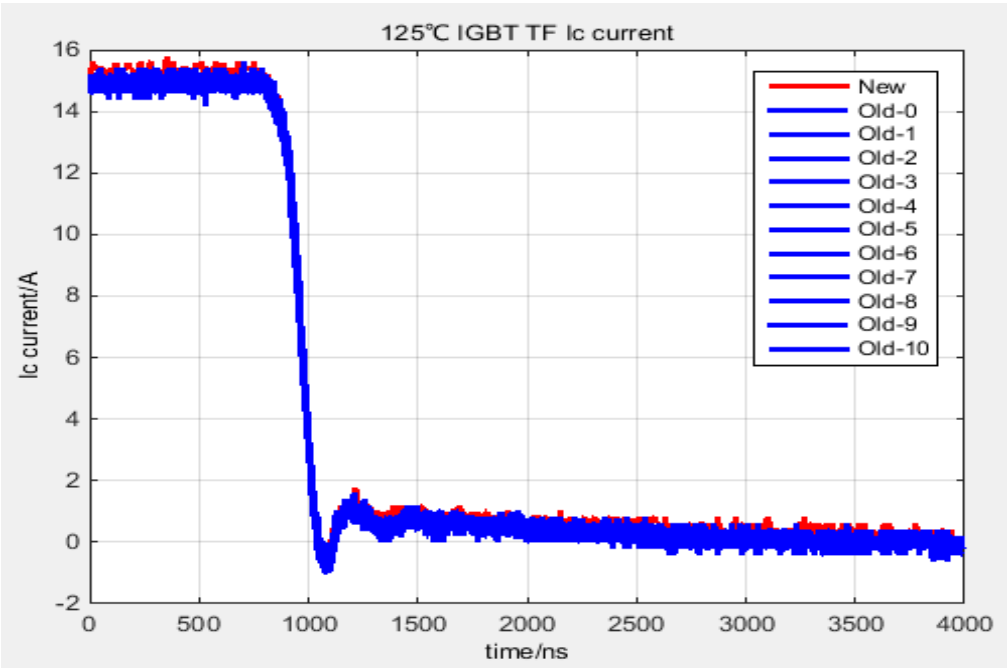


Figure 102. Inductive switching test results at 125 ℃: turn OFF IGBT Current curves.

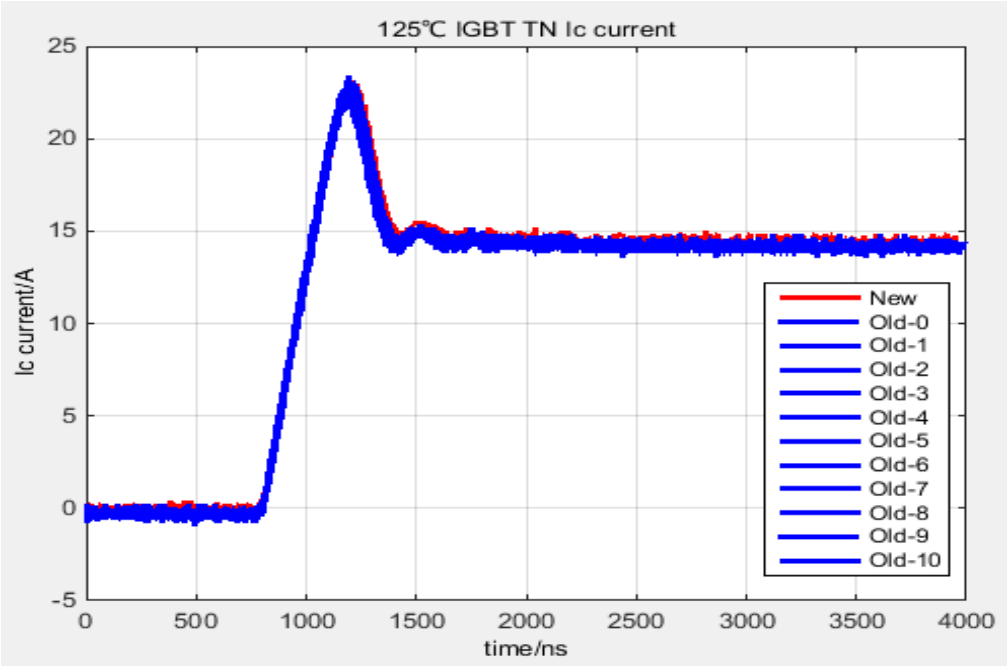


Figure 103. Inductive switching test results at 125 °C: turn ON IGBT Current curves.

Conclusion: The physical degradation of the solder fatigue does not interfere directly with the IGBT's electrical performance, so it does not cause directly increase of its power loss. Thus, degradation cannot be detected from electrical signals in such single pulse tests. However, it means physical obstruction to the removal of heat (power loss dissipation to the heat sink). In fast switching applications (e.g. converters) this will cause the T_j to rise, because the power loss or heat generated per switching pulse cannot be dispelled fast enough or as fast as before degradation. T_j has a more direct effect on the electrical power losses. It is widely documented that for the same electrical operating point (current, DC voltage, switching frequency, etc.) the higher T_j corresponds to higher power losses.

This effect can also be experimentally investigated using the inductive switching rig and thermal chamber.

6.1.2 Pulse test on larger IGBT module at different T_j levels

Experiment goal

The goal of this experiment is to observe the effect of the T_j on electrical characteristics of the large half-brick IBGT modules used in actual wind turbine converters (in the Siemens Wind Power 600kW rated converter modules that are the building blocks of their fully rated modular converters for offshore wind turbines).

Equipment list

- Inductive Switching Rig with Thermal Chamber at the School of Engineering, Warwick University – the rig includes pulse control and measurement equipment.

- DUT: Infineon half-bridge 1000A rated module FF1000R17IE4—new.

Experiment description

The DUT is placed in the thermal chamber and heated to temperature levels ranging from 25°C to175°C. Voltage and current are supplied to it from the rig using its pre-configured pulse sequence. Measurements are performed and saved using a Techtronics oscilloscope.

Experiment results and discussion

Experiment result: The effect of T_j upon the on-state voltage is not clearly visible, but this can be easily explained by fact that the current supplied to the device is very low relative to its nominal current rating. In this sense the experiment does not aim to prove the device datasheet graphs, as the current and voltage capabilities of the university rig are inadequate for the device rating.

The results show that T_j does affect the overall rise and fall-time of the signals:

- The rate of change in the turn-on current is not significantly affected, but its turn-on peak is significantly larger at higher T_j (Figure 104). The turn-off current takes longer to drop to zero (Figure 105).

- In the case of the voltage signals the rise and fall times are longer for both turn-on and turn-off events (Figure 106, Figure 107). The effect is especially visible in the reduced slope of IGBT turn-off voltage – meaning slower voltage rise.

The longer the rise and fall times of the signals (or slower rate of change) mean higher switching energy and therefore higher switching power losses.

Conclusion: This experiment illustrates the direct impact T_j has on the electrical power losses (whereas the previous experiment showed that the increased R_{th} has only an indirect impact on the losses – which can manifest only via the increase of T_j in switching applications). Thus in a converter, if higher than expected electrical losses are registered for a given unchanging electrical operating

point and cooling arrangements, this would indicate semiconductor operation at higher than expected T_j level and possible R_{th} increase. Therefore monitoring of the relative power loss increase for a known electrical operating point can indeed be used to detect degradation.

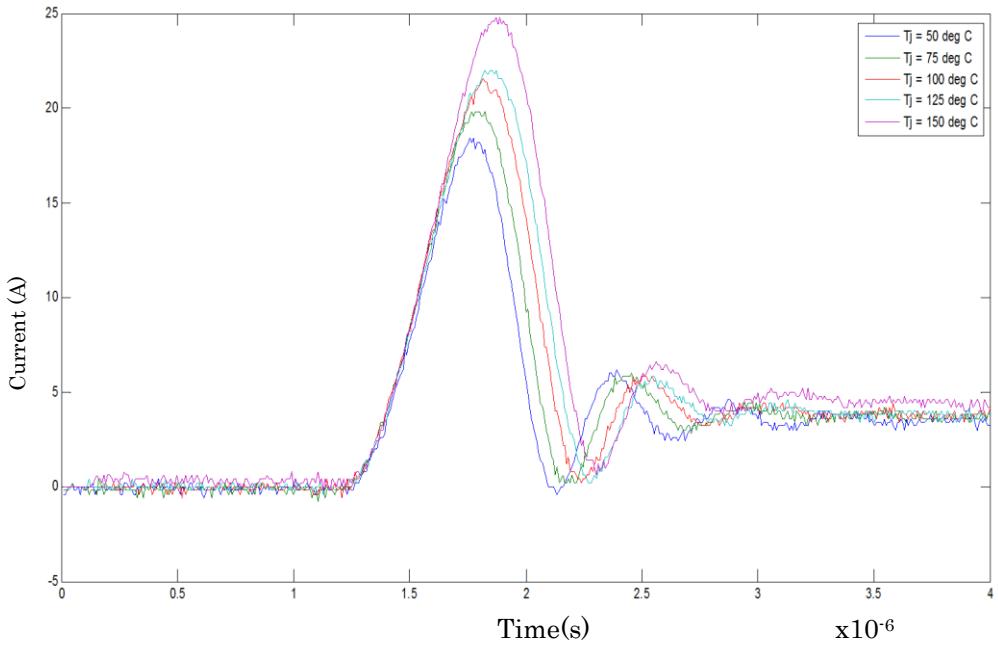


Figure 104. Inductive switching test results: FF1000R17IE4 – IGBT turn-on current.

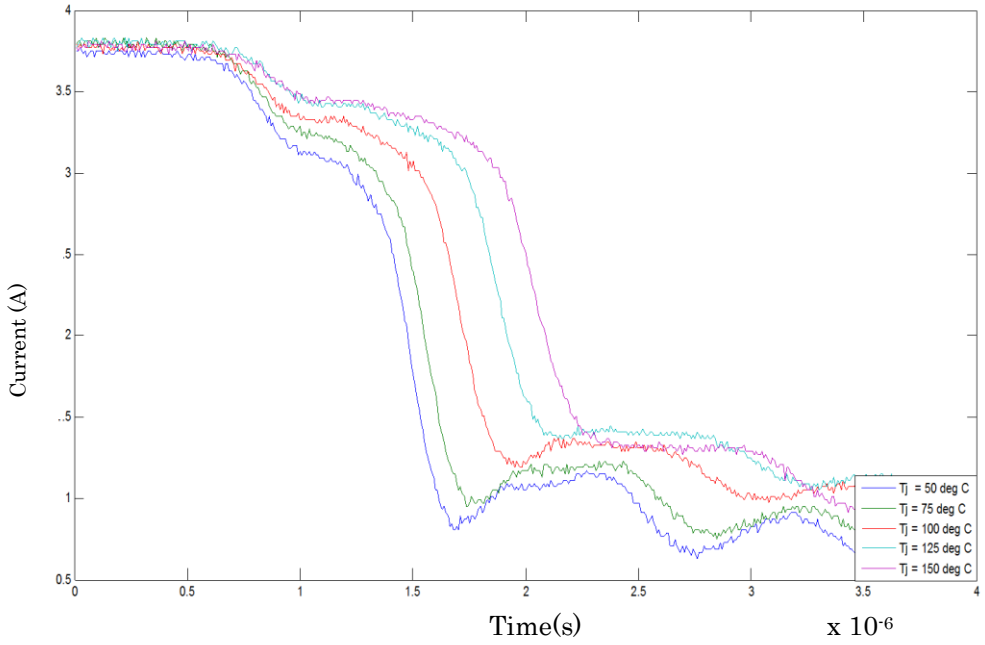


Figure 105. Inductive switching test results: FF1000R17IE4 – IGBT turn-off current.

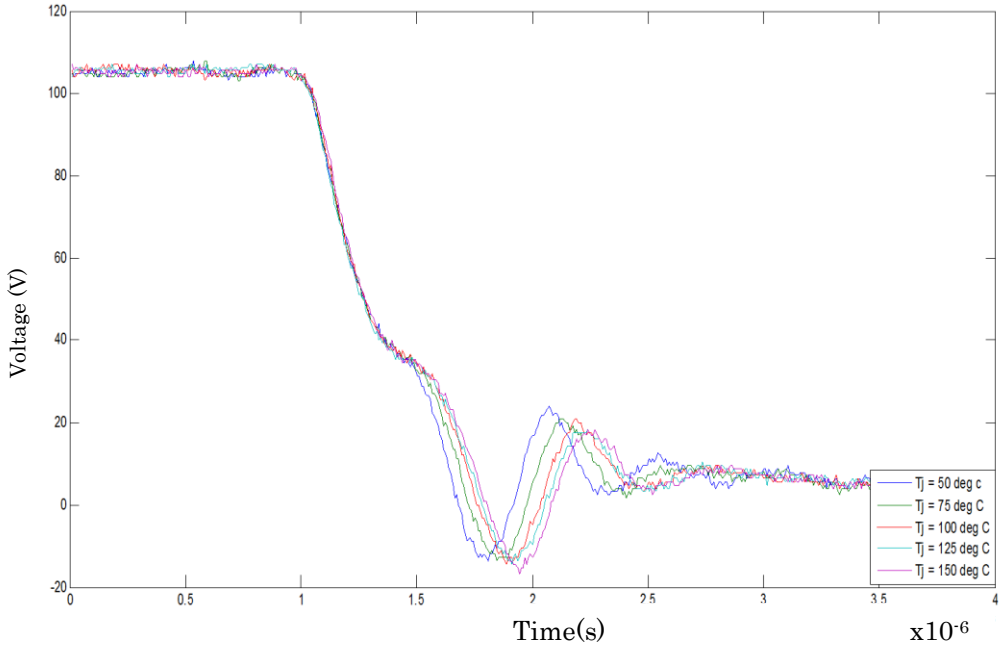


Figure 106. Inductive switching test results: FF1000R17IE4 – IGBT turn-on voltage.

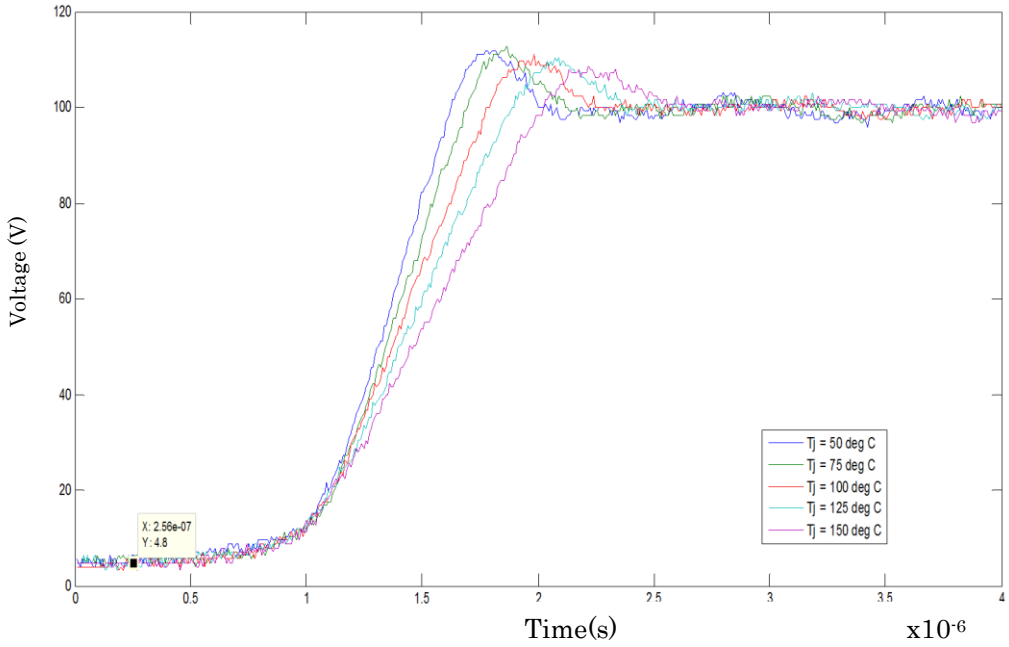


Figure 107. Inductive switching test results: FF1000R17IE4 – IGBT turn-off voltage.

6.2 ANN and Heat Sink Experiments

It was decided early in the project that analysing the device's power losses was a good approach towards building IGBT module on-line health monitoring system, as the increase of the power losses for the same electrical operating point is a clear indicator that the device is degrading and can potentially be used as an indicator of both wire-bond lift off and solder fatigue degradation mechanisms. And following this, the first experiments with the heat sink fitted with thermal sensors were aimed primarily at confirming that it is possible for us to find a reliable transfer function or thermal model of the heat sink governing the relationship

between electrical power dissipation and temperature registered by the thermocouples, which can later be used to accurately estimate what the power losses are only from the thermal signals. This is necessary since in industrial converters the I_C and V_{CE} of IGBT devices cannot be measured directly, so their power losses need to be estimated indirectly.

Thus, the aim of our early experiments with heat sources on a heat sink was to identify and test an alternative method for thermal modelling. It was confirmed by experimental observations that while lumped element thermal models such as the Cauer or Foster networks can with sufficient accuracy for 1 heat source, this will no longer be the case with multiple heat source – such as multiple chips in very large modules and multiple modules on the same heat sink – meaning that an alternative thermal modelling approach needs to be found. As the other widely used approach for thermal modelling – using finite element analysis software – is also unsuitable for on-line applications, we explored another novel option which had not previously been used for thermal modelling – the artificial neural networks.

6.2.1 ANNs and their novel use in thermal modelling

One of the major steps forward in this project was the discovery – confirmed by experiments – that artificial neural networks (ANNs) can substitute the traditional thermal models as a means for estimating power losses from temperature. Moreover, they overcome the disadvantages in terms of practical

application of the traditionally used methods. They are able to estimate power losses from more than one heat sources on the same heat sink – something with which the Foster and Cauer networks struggled – and at the same time they are much simpler than the FEA models and suitable for on-line applications.

The artificial neural networks represent a family of statistical learning algorithms based on the way a biological neural network (e.g. a brain) would function – i.e. by observing varied data input and establishing cause and effect relationships between relevant elements in it. ANNs are most often employed in the following types of problems:

- Curve-fitting;
- Pattern recognition;
- Sorting of data into categories (or clusters);
- Time sequences or trend predictions.

ANNs are used in a great number of applications in different fields of industry and science and business – a few examples of which are given below:

- Photo or image recognition (e.g. extraction of car number plates from photos, face recognition in social media applications, etc.)
- Medical analysis (e.g. deciding whether different growth samples are cancerous or non-cancerous - or sorting them into categories)
- Machine learning or the programing of computers/robotic systems to perform certain tasks by "showing" them the process

- Trend analysis (e.g. forecasting the rise of certain company shares on the stock market, etc.)
- Weather forecasting
- Human Resources management
- Data mining

They can deal with problems of highly non-linear nature and they are also used to estimate or approximate unknown functions that can depend on a large number of inputs (as is the case with the semiconductor device's power losses which are subject to a number of variable conditions defining the converter and device operating point).

ANNs are often represented as a number of interconnected layers each of which consists of a number of neurons. At minimum an ANN will have the following main components:

- An input layer – receptacle for the values of the input variables.
- An output layer – which provides the answer or result to the problem.
- One or more of hidden layers. The hidden layer contains a number of identical neurons.
- Neurons – represented identical functions – usually the sigmoid activation function. Each neuron in the first hidden layer is connected to the input layer and to each neuron in the next hidden layer, and this same configuration follows further down the line until the last hidden layer whose neurons connect to the output.

- Weights (also known as gains). They are connections between the neurons – multiplication factors which determine the proportion of the output of a given neuron which is passed on to the next layer – i.e. they indicate how important the output or activation of a given neuron is with respect to the final result. The training of the neural network adjusts the weight values to achieve minimal error in the output.

- In some cases the neural networks also include bias terms which unlike the neurons, are represented by a constant also interconnected via weight to neurons in its neighbouring layers.

- Usually the decision of how many neurons and layers are necessary lies with the creator of the neural network. The appropriate numbers of neurons and layers can vary and normally depend on the inputs and complexity of the problem. Several neural network layouts can trialled to establish which architecture provides best results.

- The training of thus defined ANN structure is governed by its learning algorithm. This is what decides the values of the weights and tunes the network to its specific future function. The learning algorithms are based on the back-propagation error. They allow the network to produce a result in the first run, check the errors between this result and what is expected for it in the output layer and the propagate it backwards in order to adjust the weights of the neurons in such a way as to minimise the error at the next run – until it reaches a point of sufficient convergence.

For the purposes of the experiments carried out during this project, a number of ANNs were created in MATLAB using the generic curve-fitting option from its neural network toolbox and their performance was tested with the experimental data. It was found that increasing the levels of the ANN above 10 and increasing the number of neuron in each layer above 15 do not improve the accuracy of the ANN and 2 layers with 10 neurons in each of them produced sufficiently good results – which was the ANN configuration used here. It takes one input – temperature – and one output – the power loss. For the input, different configurations were tried out and it was discovered than, if only one value is fed, it needs to be in the form of the delta T values (differences between the case and the chosen reference temperatures), otherwise the ANN needs the matrix of the simultaneous temperature measurements. In our trials, it was found that one significant delta T value is usually sufficient to obtain good results for the power loss of the heat source. Datasets of around 3000 dta point were used for the training of the ANNs and they were then tested with different datasets of varying length. The training algorithm used was the Levenberg-Marquardt as it was found by trial to produce the closest fitting ANN result.

Once the a neural network is trained for a given set of conditions and deployed, it does not change any further – its weights are then set values (this applied at least in the case of the thermal networks with which we experimented here). Thus, if the system it models is experiences any significant changes which

have not been previously factored into the training process, the ANN may not be able to output correct results.

In the heat sink experiments conducted here, for any change made in the thermal system, such as the addition of a heat source or water cooling, a new ANN had to be created. In view of practical applications this simply means that any ANN training must be done on the complete thermal system as it is or will be operating in the field. While the whole condition monitoring system can be generic and suitable for deployment with different converters, the ANN training itself must be specific to the deployment conditions in every single case. Once calibrated to a specific converter the ANN algorithm's output may not be valid for another converter, but this should not necessarily be considered a shortcoming if the condition monitoring system is implemented as a part of the converter control and not as a stand-alone unit.

6.2.2 Cold plate and heat source experiments

The bulk of the experiments conducted during this project use an aluminium body cold plate with 4-pass inlaid copper piping manufactured by Aavid Thermalloy. Schematic drawing of this heat sink is given in Figure 108 below. The aim of the early cold plate experiments was to observe how the electrical power losses manifest as heat from the point of view of the heat sink. The choice of the cold plate (instead of a still air convection cooled heat sink as used in the

COMPERE project) is based on the fact that the heat sinks used in offshore wind turbine converters are predominantly liquid-cooled.

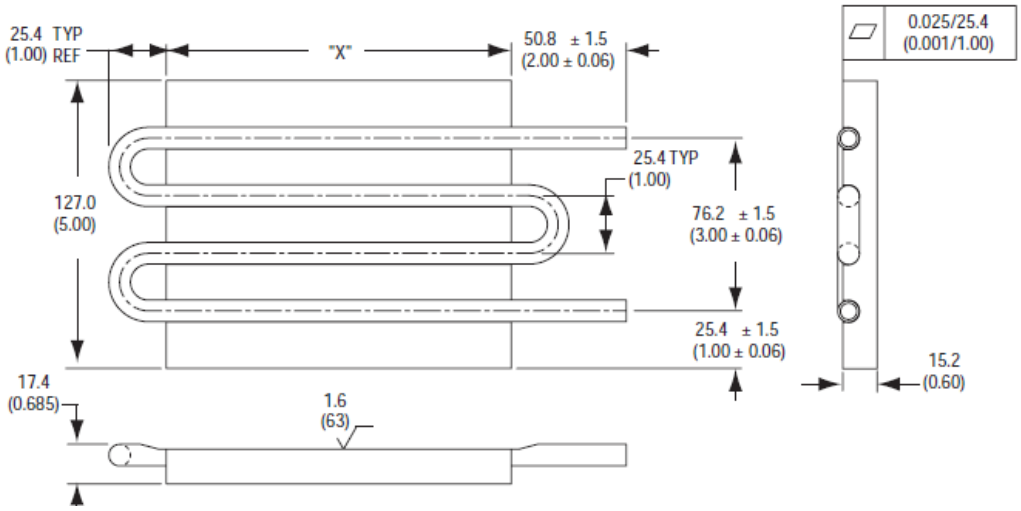


Figure 108. Aavid Thermalloy cold plate schematic drawing with dimensions.

The heat sink was prepared for the experiments by drilling module mounting holes (threaded) and thermocouple mounting holes through its body. Figure 109 below shows the heat sink with mounting holes drilled in it and a blow-up of a thermocouple mounted through the heat sink body. The thermocouples used were a standard K-type. They were secured using thermally conductive self-shimmying glue paste following good practices guidelines for thermal measurements. Five thermocouples were mounted through the heat sink body with their tips exactly on the surface, i.e. right underneath the base plates of any mounted heating elements.

Figure 109. Preparation of cold plate for thermal experiments.

A number of other thermocouples were fixed using the same paste on opposite surface of the heat sink – as shown in Figure 110. Some were placed directly next to the entry points of the first through-mounted thermocouples, so that the top and bottom thermocouples can measure the temperatures across a short and simple 1D heat flow path through a single medium (the aluminium material of the heat sink body) – as shown in Figure 111 – with the intention to try and use simpler transfer functions for thermal modelling (such as Cauer and Foster ladders). Another few thermocouples were glued close to some of the edges and corners of the heat with the intention to try using some sort of matrix of thermal measurements to develop the heat sink thermal model for to estimating injected electrical power losses.

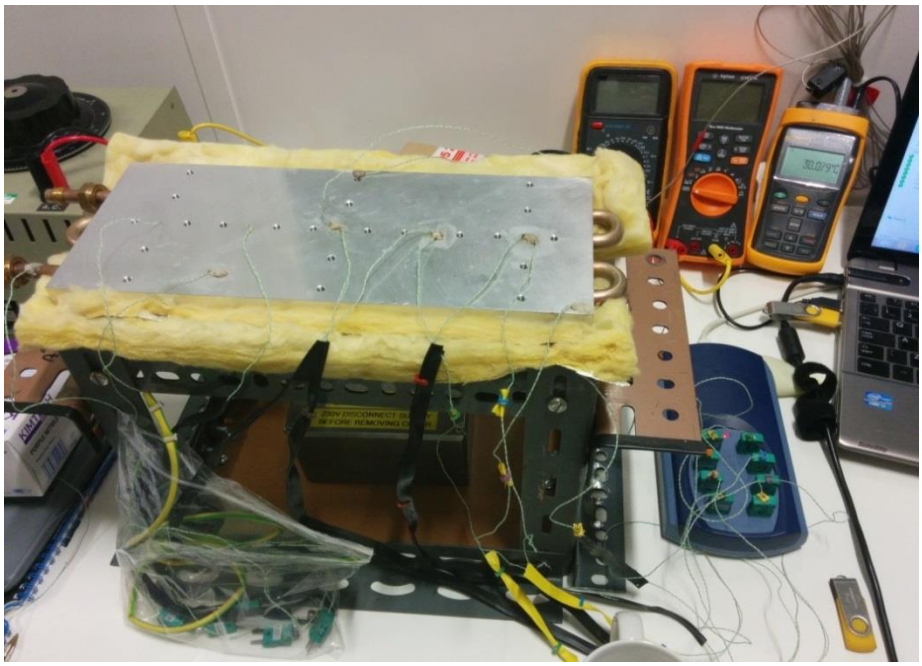


Figure 110. Heat sink bottom surface showing the thermocouples placement.

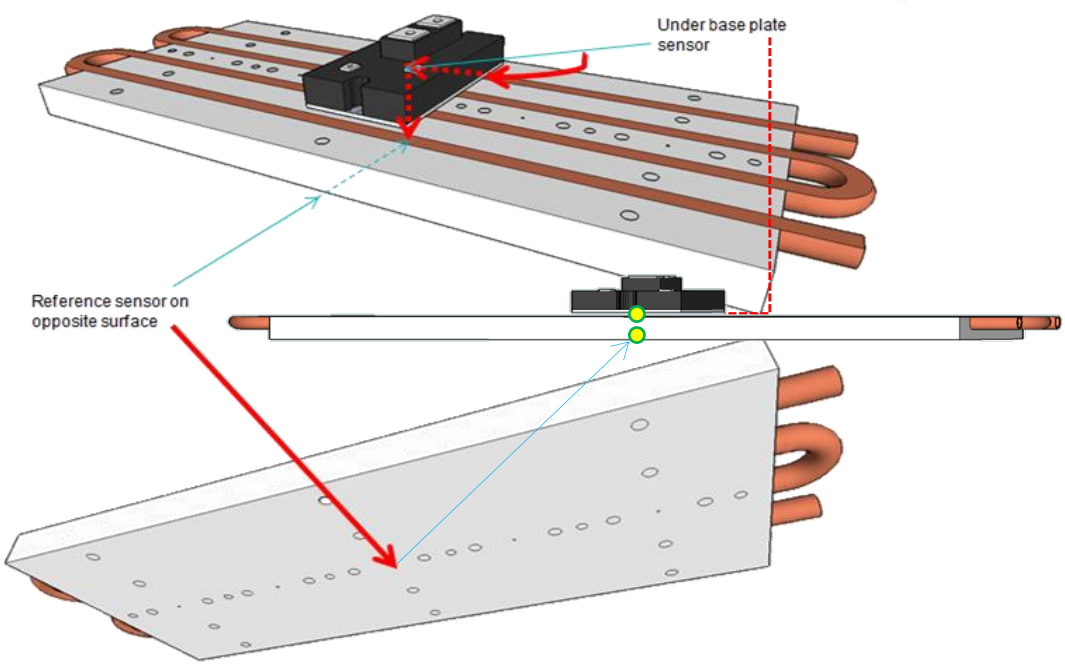


Figure 111. Thermal measurements across a simple 1D heat flow path.

Initially the response of the dry heat sink was tested (as shown in Figure 112) as it was suggested that this may be important for building the heat sink thermal model.

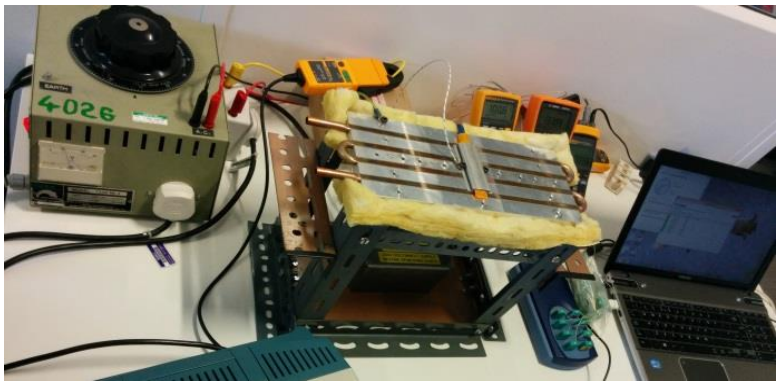


Figure 112. Dry tests with a heating device (HP06 DBK).

It was found that when dry its thermal time constant is in the range of hours – as can be seen in Figure 113 below.

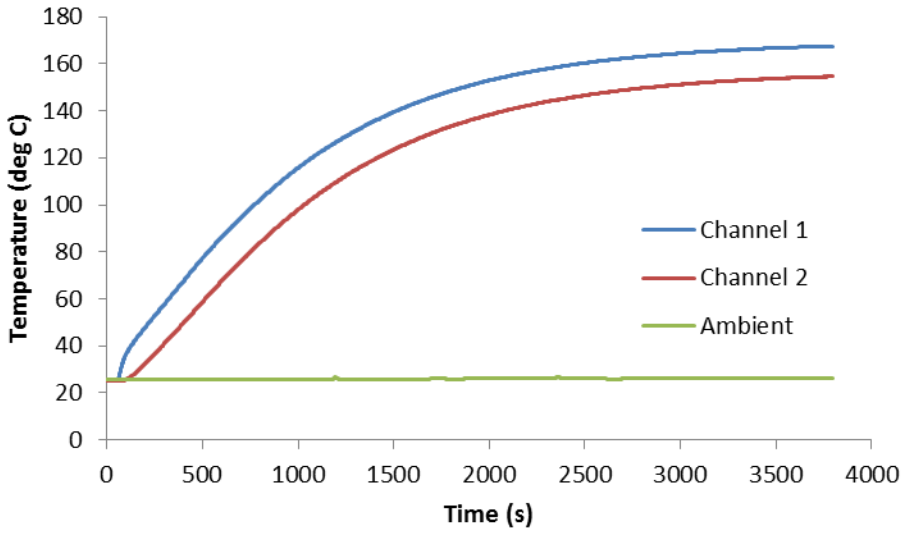


Figure 113. Thermal response of the dry Aavid Thermalloy heat sink to a power step of 220W.

In the majority of the early experiments with the cold plate high power dissipation resistors (Vishay Resistors LPS 300) were used as heat sources, as we simply wanted to inject electrical power losses into the heat sink, regardless of their source, record the change in temperature signals as a result of that and try to find a model describing the correlation between the two phenomena. Four kinds of experiments were carried out: a/one heat source on the dry heat sink, b/two heat sources on the dry heat sink, c/one heat source on the heat sink connected to a water chiller (LAUDA WK3200 – providing flowrate of 0.11 l/s and internal water temperature regulation with an accuracy of about 2 ° C), d/two heat sources on the water-cooled heat sink. All of them followed roughly the same experiment procedure consisting of the following steps:

1. Securing heating resistor(s) on the heat sink and starting the chiller in the water-cooled experiments;

2. Supplying varying levels of voltage to the heating element(s) within the rating of the heating element and power supply;

3. Recoding the voltage and current of the devices and the temperature readings from sensors placed on the heat sink body, (as well as the ambient temperature);

4. The current and voltage were used to calculate the electrical power loss of the heating element.

5. Carrying repeating the above steps in a new round with new power loss injection sequence.

6. This power loss from one or more experiment rounds together with its corresponding set of temperature measurements were used to create and train an ANN.

7. The ANN was then tested with the temperature set from another experiment round to check whether the result will be a close match the measured electrical power.

A custom-made DAQ virtual instrument using the LabVIEW platform was developed for the combined data acquisition of the electrical, thermal and – with the connection to the water chiller– also the flow rate sensor counter signals. Due to the practical limitations imposed by the DAQ rate of the temperature datalogger (PICO TC-08), both electrical and the thermal signal signals were acquired at 1 Hz.

The figures below show sample results from the early heat sink experiments with ANNs. At this stage the focus was on demonstrating the ANN's general applicability for the intended use (i.e. that its output can follow the shape and amplitude of the measured power), not on minimising the error of its estimate, which was within 8% mean square error.

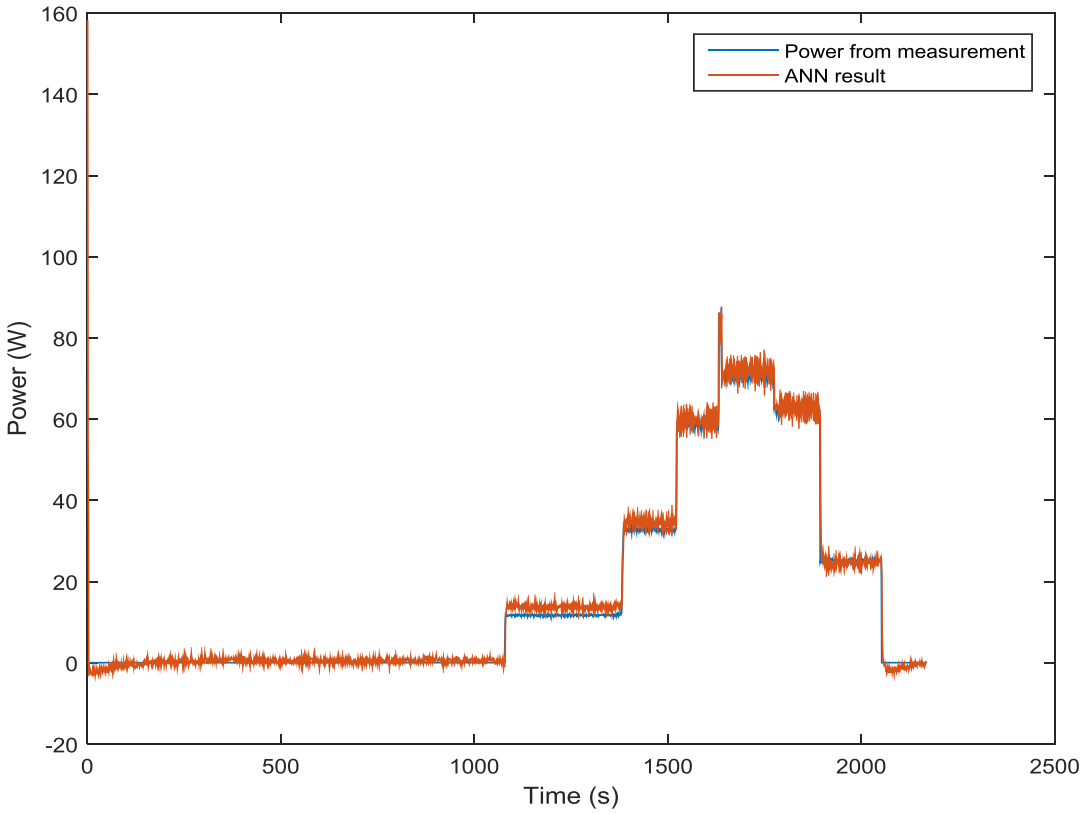


Figure 114. Example result from the dry heat sink tests with a single heat source.

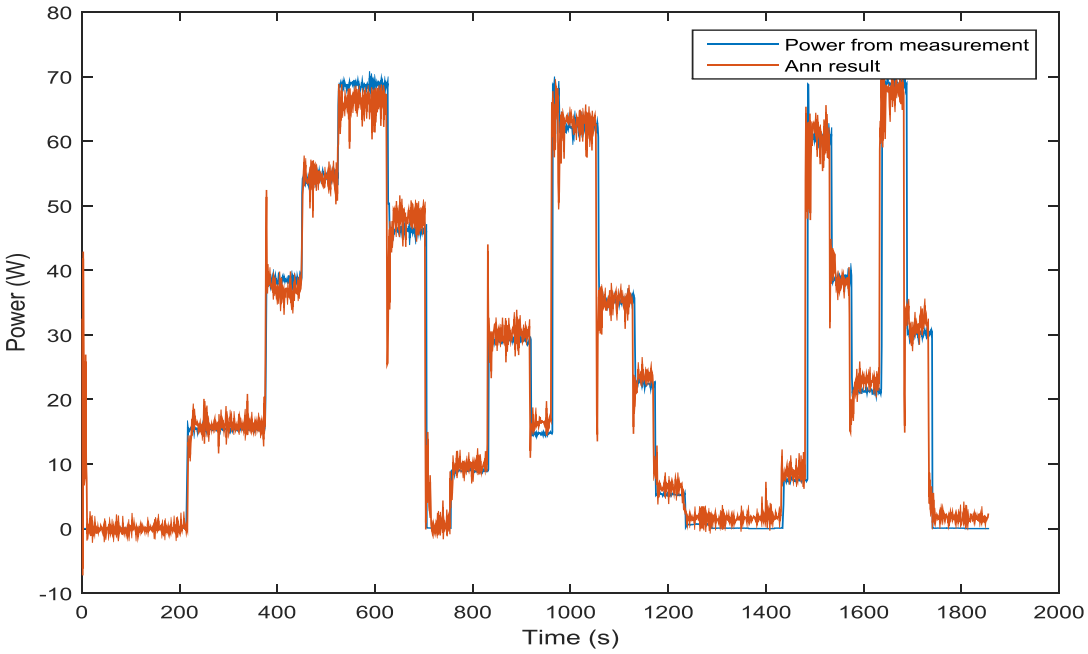


Figure 115. Example results from the dry heat sink tests with double heat source – ANN power loss estimation for resistor 1.

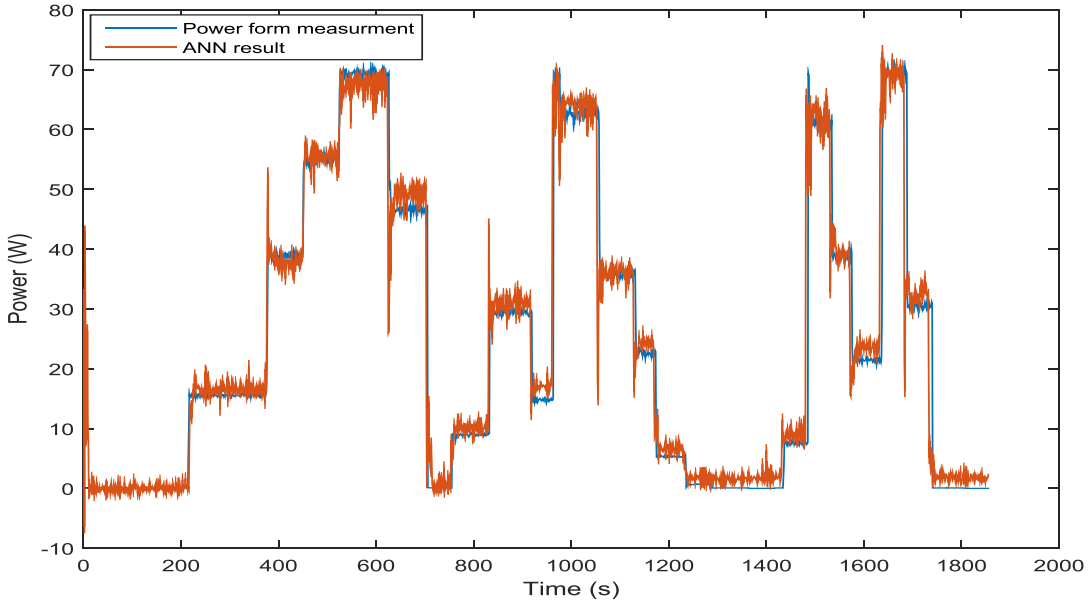


Figure 116. Example results from the dry heat sink tests with double heat source – ANN power loss estimation for resistor 2.

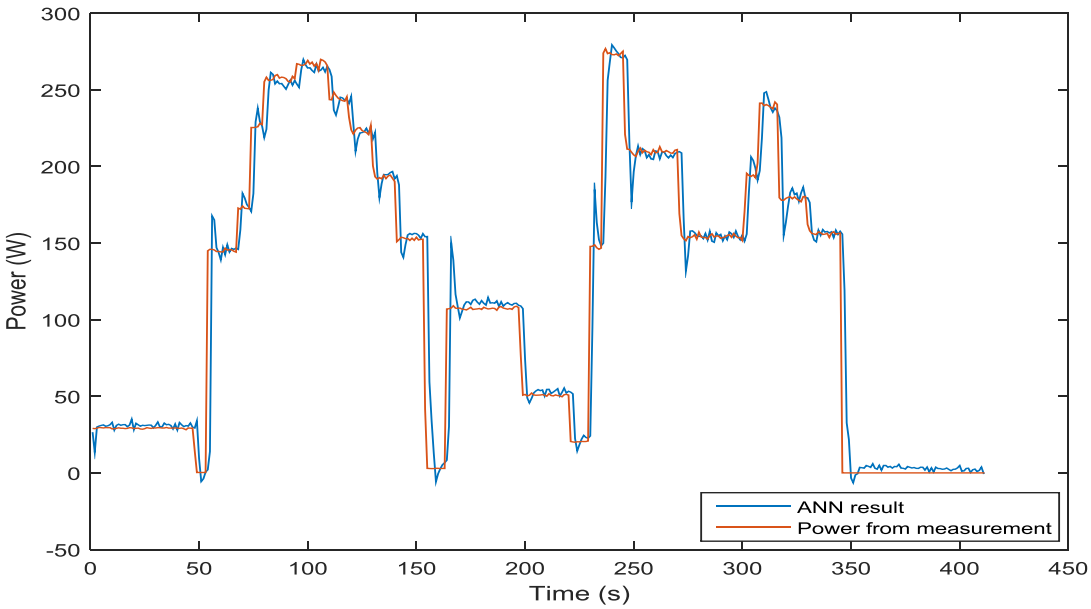


Figure 117. Example result from the water cooled heat sink tests with a single heat source.

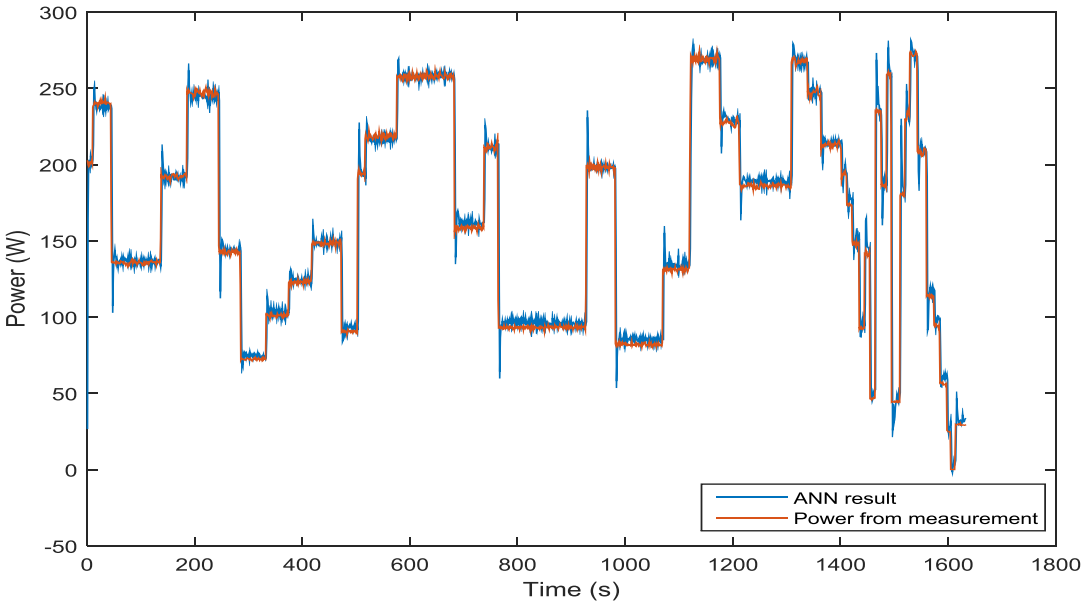


Figure 118. Example result from the water cooled heat sink tests with a single heat source.

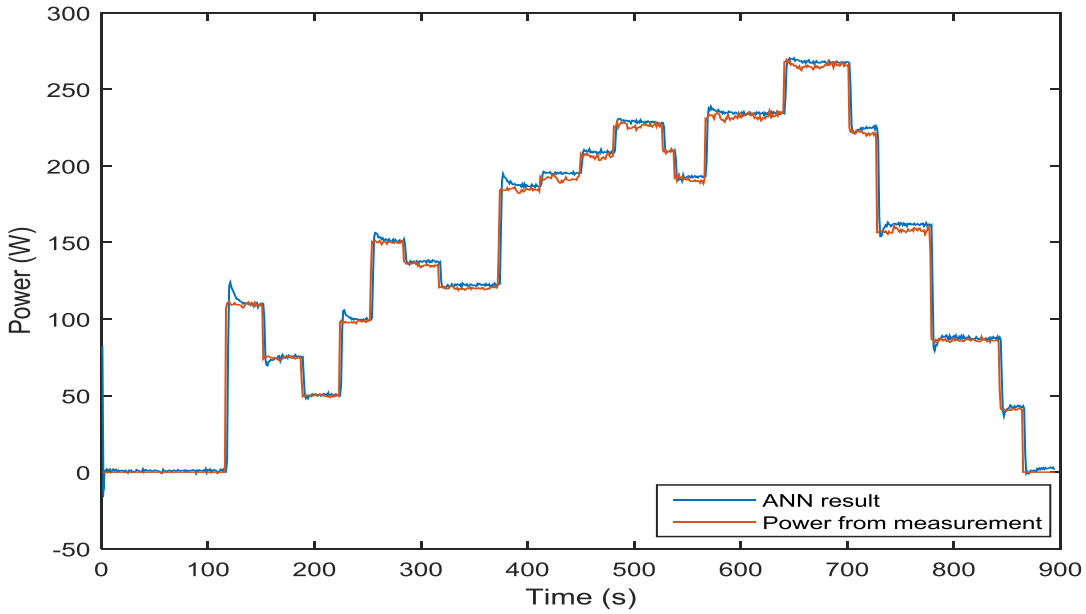


Figure 119. Example results from the water cooled heat sink tests with double heat source. ANN estimation of the power loss of resistor 1.

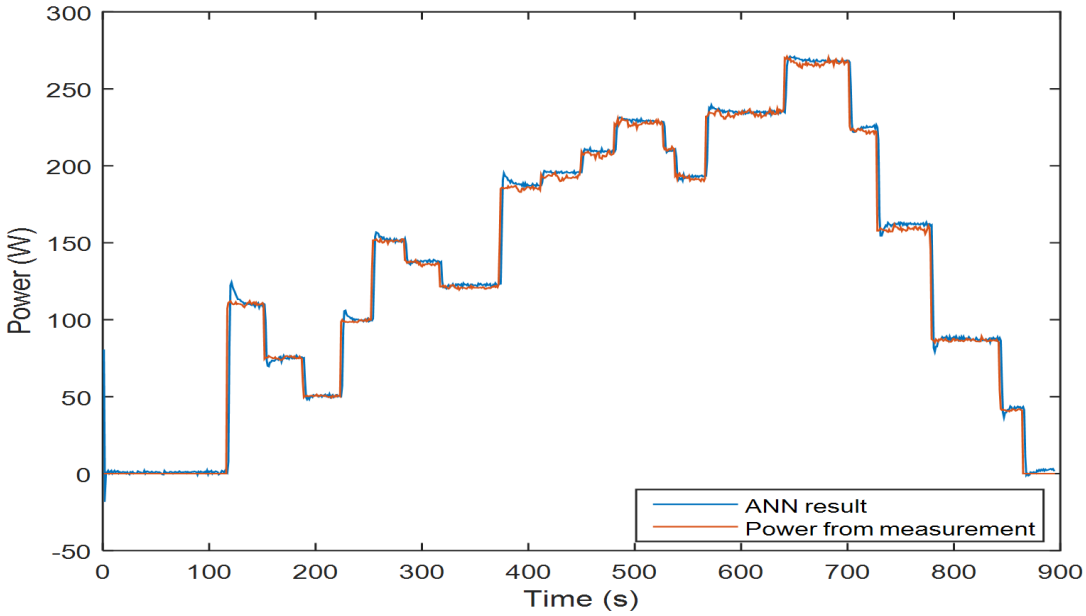


Figure 120. Example results from the water cooled heat sink tests with double heat source. ANN estimation of the power loss of resistor 2.

6.2.3 Thermal experiment observations

A few practical observations were made in the process of experimenting with the cold plate which it would have been difficult to deduce otherwise.

- It was found that the best temperature to power correlation was achieved by the ANN when it was fed not absolute temperature (direct channel readings), but differences in temperature between the channels (referred here as delta T and obtained by subtracting the reading of a channel from the reading of another selected channel). This is explained with the fact that the very definition of losses dissipated as heat includes a point-to-point temperature difference term. Although it is possible for an ANN to factor in this comparison between the values of its input matrix, it was easier to train ANN.

- Fluctuations in the water temperature (due to the periodic start of the compressor of the secondary loop of the chiller) were observed in all experiments with water cooling. However they did not affect the results due to the fact that not absolute temperatures but temperature differences were used as inputs to the ANNs, and those fluctuations were captured in equal proportion by all heat sink attached thermocouples.

- It was found that the best temperature to power correlation was provided by the difference not between the case and ambient as suggested by the COMPERE results, but between the case and a reference point on the heat sink body. Of all possible delta T combinations, the delta T from the readings of the case sensor and

the sensor directly across it on the opposite surface of the cold plate was found to produce the closest fit between power estimate and measured power. It represents a simple straight heat flow path through a homogenous material, avoiding the uneven rate of power dissipation which can occur with the change of medium or the change of heat transfer mechanism (i.e. conduction to convection, if the case-to-ambient delta T is used).

- Using the delta T between the case and a reference point directly across the heat sink has one very important benefit over the case-to-ambient delta T – a much shorter time constant. It allows the temperature curve to follow more closely shape of the power loss as illustrated by case B in Figure 121. In case A one simple step in power needs to be matched to a complicated temperature curve – i.e. to estimate one power value we will need to consider a long sequence of different temperature values.

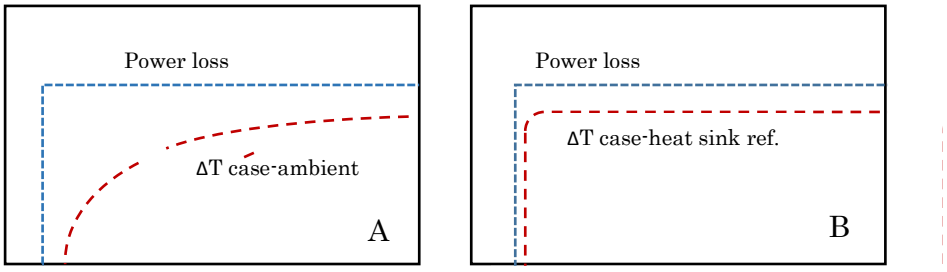


Figure 121. General comparison between case-to-ambient and case-to-heat sink reference delta T waveforms.

With quick changes in power, the whole temperature sequence (from beginning of change to steady state) will not be available and the portions of it that

are will be affected by previous power conditions, and thus produce large error in the power loss estimate.

- The time delay between the ANN power estimate and the measured electrical power was around 20 seconds in the case of the "dry" heat sink tests and below 3 seconds in the case of the tests with water cooling. Thus, the fact that larger wind turbine converters use liquid cooling systems will be to our advantage in terms of the practical application of the health monitoring concept we are working on in this project. The further work with IGBT modules is done only with water-cooling.

- Another important finding was that the position of the heating element on the heat sink matters with respect to the temperature rise observed from the same power loss. In the case of our heat sink, when the heating element was mounted in centre position on the heat sink it displayed higher case (and delta T case-to-heat sink reference) temperature than when it was mounted in end position. The same applied when two heat sources were used both dissipating the same electrical power loss: the one in the centre always had higher case temperature than the one at end position. This is important because even though the heat sources and their power losses are exactly the same they cannot be modelled by the same thermal model – it demonstrates why the junction-to-case Foster models provided by the manufacturers cannot provide accurate results. Cauer networks are also unable to account for this effect of the position. ANNs can overcome this issue, but only provided they are trained with multiple temperature signals including case signals

from each individual device. ANN trained on a given type of module cannot be used for this same type of module (even the same module itself) in a different heat sink position. This is important to know for the practical application of temperature based health monitoring.

Overall, the initial experiments with the heat sink and heat sources provide some valuable first hand lessons about the behaviour of thermal systems similar to the ones we aim to monitor in wind turbine converters. The results from the power loss estimation using ANNs are also promising. They demonstrate that an ANN is capable of:

- Performing backward correlation of temperature signals to power loss with sufficient accuracy. The early experiments with ANN showed a mean square error of 8% or below. During this stage the aim was only to demonstrate that the ANN output follows the same pattern as the measured power loss – something which the ANNs accomplished which well. This indicating that improvements in their output accuracy, through changing the parameters of the used ANN or fine-tuning is also achievable.
- Accepting multiple temperature inputs to model one or more power loss sources simultaneously. In the early heat experiments, this capability of the ANNs was tested with the one and with two physical heat sources mounted on the heat sink. In the first case, an ANN was created with one input and one output and in the second case, an ANN was created with two inputs and two outputs. In fact, the input to the ANN can be seen as a matrix. It can contain a single delta T value for

modelling the power loss of one heat source, or several temperature values for modelling the power losses of several heat sources. This makes the ANNs in general a flexible tool for modelling multiple power losses occurring in parallel. However, the input matrix of the ANN must contain consistently the same number of elements as the input with which the ANN was generated and trained. Thus, new ANN needs to be created when heat sources and sensor channels are added or removed from the system. Nevertheless, since converter topologies and the number of power modules they contain is fixed, this will not be a problem.

- Learning from real-life experience. The ANN can be trained during early deployment stages to capture the healthy power loss signatures of the new devices operating without degradation. Thus, the model it in effect represents will be based on the real-life conditions the device experiences in its day-to-day operational life (the cooling arrangements, the control system, the ambient conditions, etc. – all of which are important, but hard to facture in a thermal model of the device on its own as can provided by manufacturers).

ANNs can provide a useful alternative to thermal modelling for the purposes of semiconductor power loss estimation in frequency converters. Although once trained an artificial neural network would be converter specific, the ANN architecture and training algorithms can be generic, thus they can be added as a standard feature to the converter controller (within a complete power module health monitoring package) and the training can be programmed to happen automatically after deployment in the field.

6.3 Experiments with IGBT Modules

After the ANNs were identified in the earlier round of experiments as a suitable tool for practical power loss estimation, it was necessary to see how would perform with actual IGBT modules. The new round of experiments used the widely commercially available SKM50GB12T4 half-bridge modules in place of the previously used resistive heat sources. The experiment set-up included the same cold plate and water chiller and the same sensor and DAQ arrangements. In this experiment the IGBT devices with their gates permanently open (at 15 V gate voltage potential supplied by smaller voltage source) were connected directly to a current source capable of delivering their rated current (Sorensen DHP 15V/1320A). The IGBT on-state voltage and current were measured and datalogged together with thermocouple readings and then used to create ANNs. Only the top IGBT chip of the half-bridge was used in this experiment (the case temperature sensors were directly under the location of the chip). When two modules were used simultaneously, again only the top IGBT chip in each module was active.

Experiments were conducted with both healthy and degraded devices in different positions on the heat sink. As previously observed the heat sink position resulted in different case and delta T case-to-heat-sink-reference values. Figure 122below shows the delta T curves of two brand new devices (as unpacked) with the same on-state power loss. One was mounted in the middle of the heat sink and the other – in an end position.

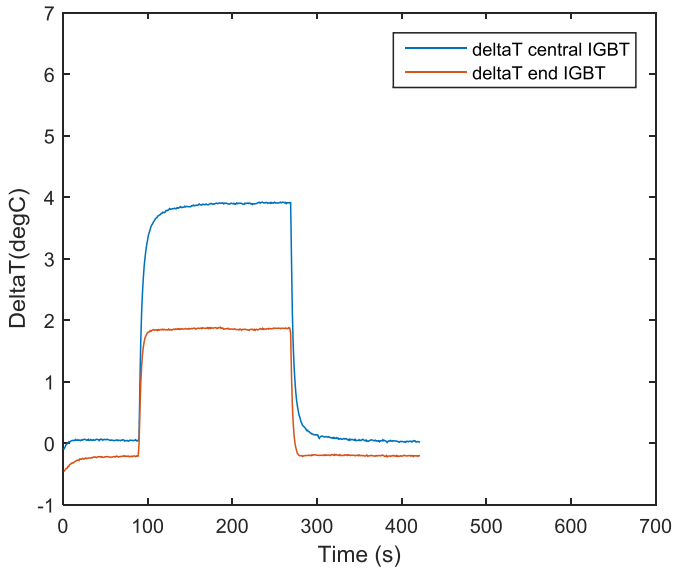


Figure 122. Delta T case-to-heat-sink-reference for two healthy IGBT devices.

The module positioning is illustrated by the image below (Figure 123).

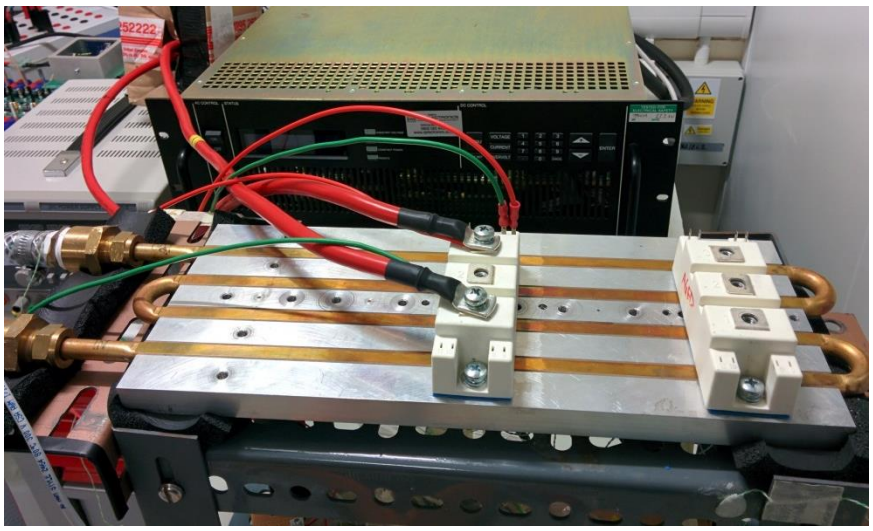


Figure 123. Centre and end module positions on the cold plate.

Many experiments were conducted with healthy and degraded IGBTs used as single heat sources in both center and end positions and as double heat sources in a variety of position combinations. The healthy IGBTs were new unused devices, while the degraded IGBT had undergone substantial power cycling (up to 70,000 cycles at large ΔT_j amplitudes of around 70-80K). The results of these experiments can be summarised as follows:

1. ANN trained with a power and delta T dataset obtained from healthy IGBT (acting as single heat source) can estimate the power losses of other datasets obtained from healthy IGBTs in the same position (either centre or end). But it cannot accurately estimate the power losses from a degraded IGBT in the same position.

2. ANN trained with dataset obtained from a degraded module can estimate the power loss from other dataset of the same degraded IGBT in the same position. But it cannot estimate the power loss of other differently degraded IGBTs, nor the power loss of a healthy IGBT.

3. In the case of double heat sources similar rule applied – the ANNs were accurate only if used with another dataset of the same kind of module (healthy or degraded to the same extent) and in same heat sink positon.

To find out why the ANNs could not model well modules with a different health state, we looked at signals used in the creation and training of the ANNs: the power loss which heats the module and the resulting delta T rise (taken as specified above, across the thickness of the cold plate directly under the module).

The power and delta T curves of one healthy and three degraded modules are compared in Figure 124 and Figure 125 below. They were obtained for 2 heat sink positions (the centre of the heat sink and the end of the heat sink), with all modules mounted and tested one after the other in the same position. It was observed that the position affects significantly the delta T signals. Figure 124 gives the signals obtained at the central position. As expected, the healthy module has the lowest power loss and the lowest delta T change respectively. The other three modules display almost the same level of power loss. From this it can be expected that their delta T curves should also show very similar levels of rise, but in fact they are noticeably different. While in this case the delta T curves of all three degraded modules remain higher than that of the healthy module for the same power loss level, it can be seen that delta T of degraded module 2 is very close to that of the healthy module, while module 7 is consistently higher and remains around half-way between the delta T of module 2 and the delta T of module d – the highest in this set. This incongruity becomes even more pronounced at the end position on the heat sink position – as can be seen in Figure 125.

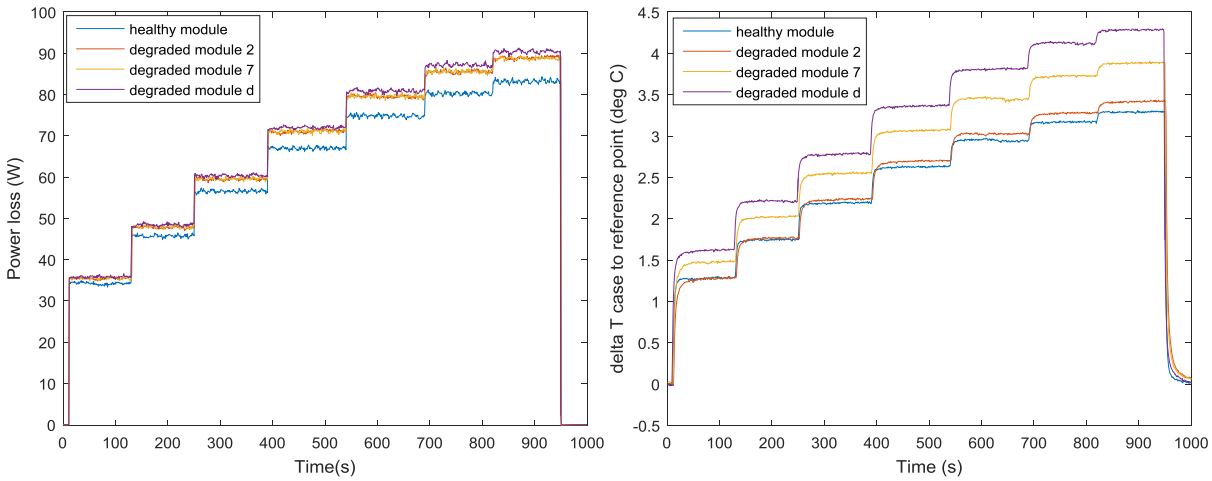


Figure 124. Power loss and corresponding delta T change in the central heat sink position.

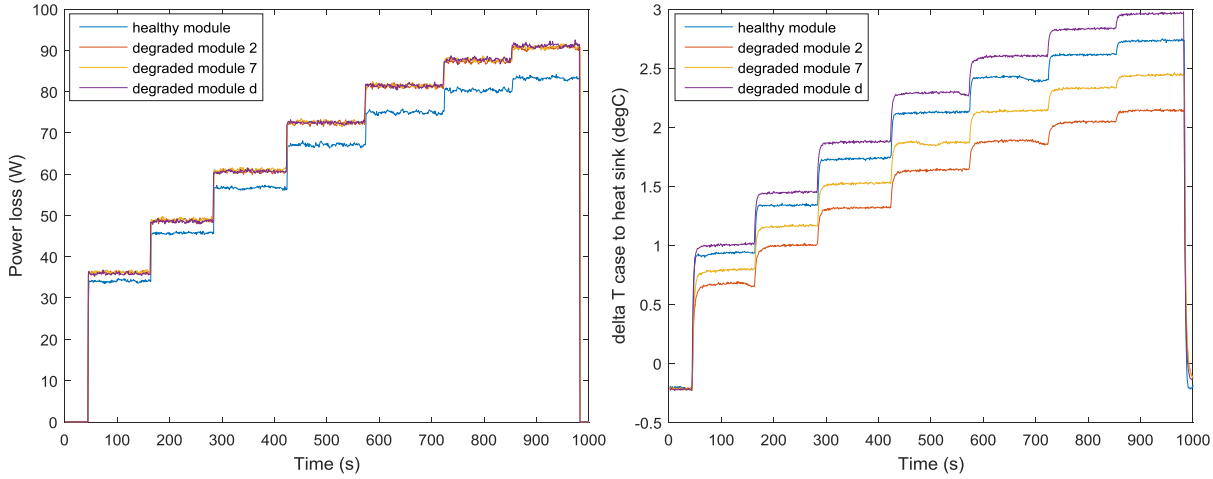


Figure 125. Power loss and corresponding delta T signals of the same modules in end position on the heat sink.

Logically, the power losses of the modules are the same as registered previously – with the healthy module displaying the lowest and the three degraded

modules having almost the same level of conduction loss. In this position however, the delta T curves of degraded modules 2 and 7 are now surprisingly lower than that of the healthy module. Only the delta T of degraded module d remains consistently higher with respect to the healthy module signal (as does its power loss curve).

These discrepancies may be due to different levels of degradation, different degradation mechanisms, or a combination of both. Further scans or destructive opening of their packaging may be needed to establish the exact reason for their thermal behaviour described above. Still, this is empirical evidence that reaffirms some of our previous observations:

- The physical position of the module on the cold plate matters.
- A difference in the external cooling environment of the module can change its observed thermal resistance R_{th} along a given heat flow path.
- This can either allow more heat along this path or divert some of the heat flow along a different route.
- Thus for the same power and the same segment of the given heat flow path we can still observe different temperature rise depending on how the heat flow was redirected under the combined influence of the R_{th} and the cooling system before the points of measurement.

Working with actual degraded IGBT modules can be very challenging, especially since we don't know their degradation mechanism, stage of degradation and remaining useful life, but it gives all the more value to our search for a

practical IGBT health monitoring solution. After all, in the filed we are not going to have that information about the IGBT modules we will be trying to monitor.

Our initial idea was that an ANN can be created and trained in the field with data from the new and still healthy device. This ANN will then be used to estimate the module power losses throughout its lifetime and if those losses start to increase for a given known operating point, this will signify that degradation is in progress.

This approach seemed justified, since the ANNs for the IGBT modules will be trained at the exact same condition that the devices will operate. The position of the IGBT on the heat sink will be fixed, the heat sink itself will not change, etc. However, the above data shows that as the IGBT module degrades its internal thermal system may change significantly. Thus, the ANN created and trained to model the behaviour of the healthy device can later become invalid and produce wrong power loss estimates.

Figure 126 provides an example of such inconsistent loss estimate for 4 IGBT modules. The ANN used was trained with data from the healthy module, and thus it can provide a fairly good estimate of the healthy module power losses when fed delta T data for it. For the other two modules – degraded modules 2 and 7 – the ANN predicts power losses than they actually experienced and for the degraded module d, the estimated losses are very slightly higher than the actual one.

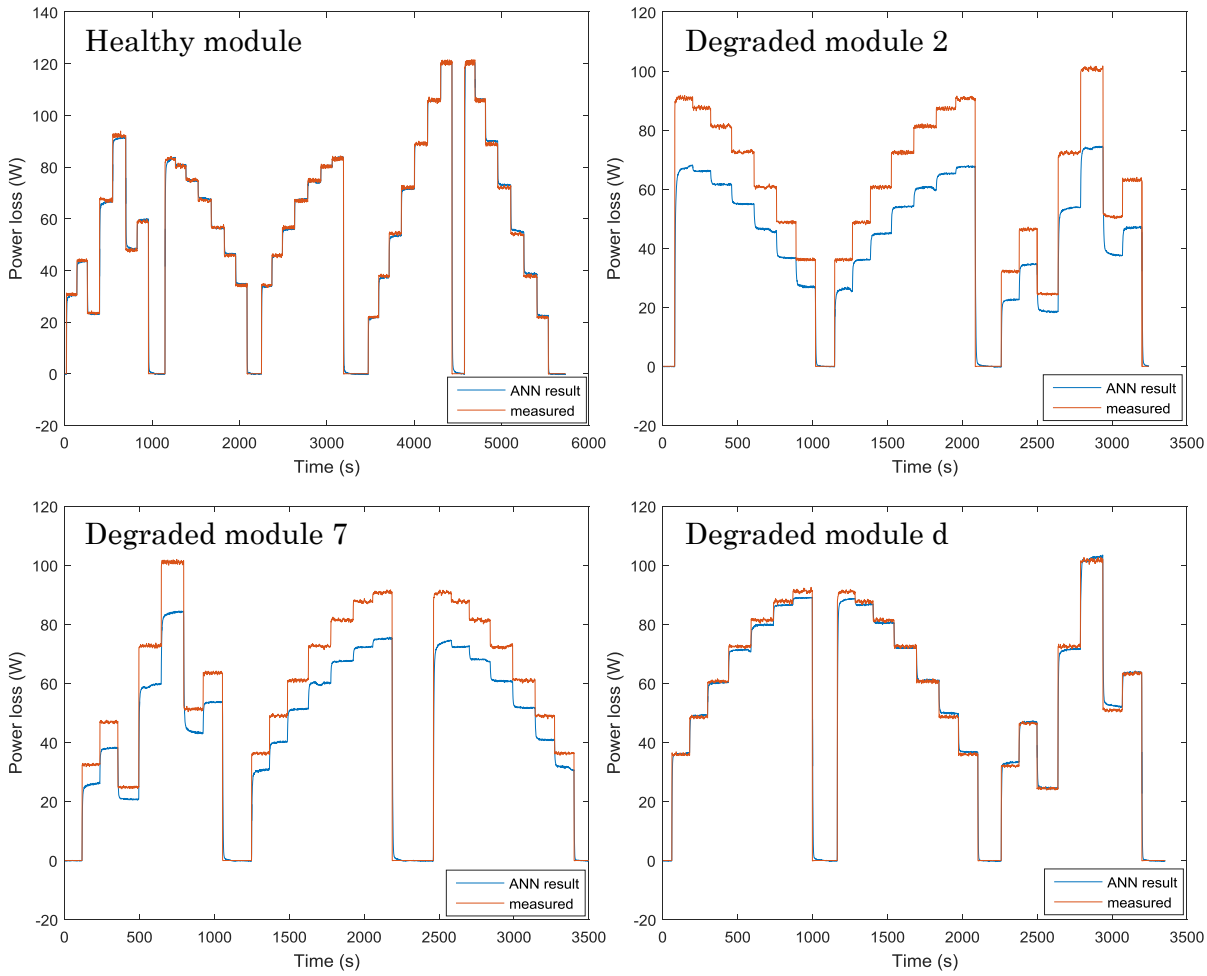


Figure 126. Power loss estimate using ANN trained with healthy module data and applied with the healthy module, degraded module 2, degraded module 7 and degraded module d (in centre-position).

.

The module with the best power loss estimate is the one upon whose data the ANN was based. Similarly, if the ANN is trained with data from module d, it will produce a reasonable estimate of that module's power loss and again much poorer estimate for the other 3 modules.

The same happens with the estimates of the power of systems including two modules simultaneously experiencing losses. If delta T and power data from a system of two healthy modules is recorded and use to train ANN for their power losses, this ANN can further estimate fairly well the power losses this particular system – as seen in Figure 127 below. The estimate is noisier than in the case of one single module, but it does follow the trend of the actual power loss.

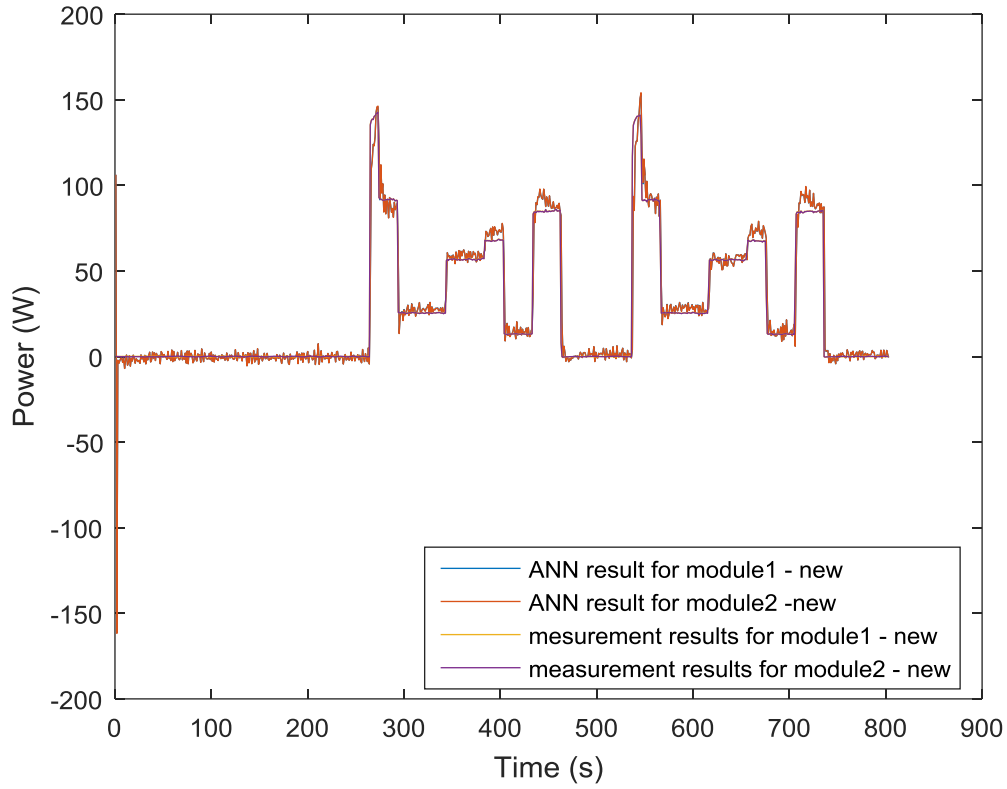


Figure 127. Experiment with two healthy modules

If an ANN is created for a system with one healthy and degraded module (, again it will be able to get a good estimate of the power loss of this system only based on temperature reading from it.

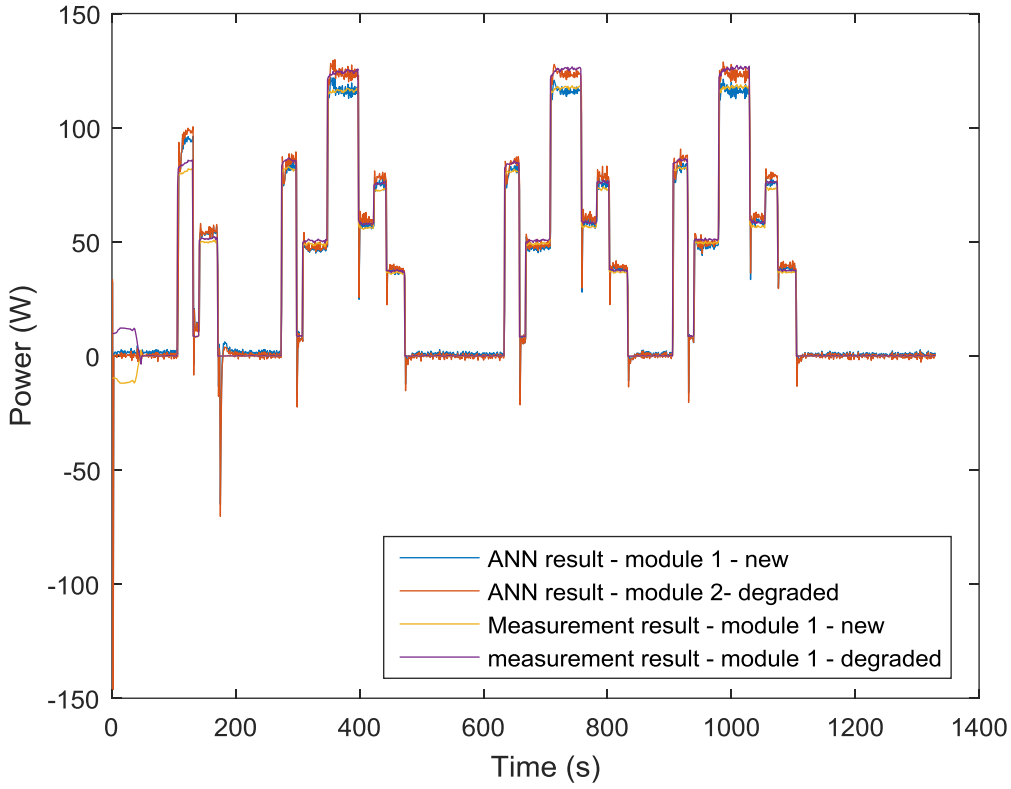


Figure 128. Power estimate by ANN trained with a system with one healthy and one degraded module and fed further thermal data for that system.

However, if we use the ANN trained with the fully healthy system (with 2 healthy modules) and apply it with the system where one of the modules has degraded 9as is likely to happen in real life) the estimate error will be very large – as seen in.

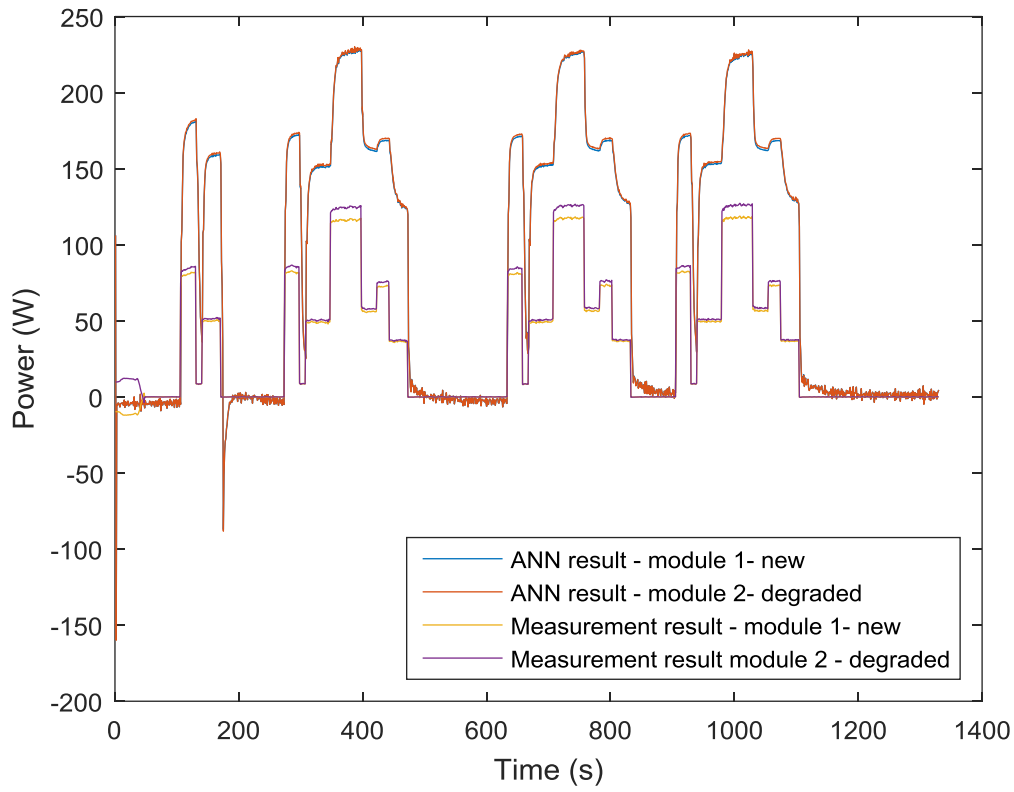


Figure 129. ANN originally trained with data from a system with two healthy power modules applied to a system with one healthy and one degraded module.

Figure 130 below provides another example of a mismatch between the actual power losses occurring in a severely degraded module and the ANN estimate for these losses. In that example, because of the quicker changes in the power steps (and its corresponding delta T signal which has less time to reach steady state), the ANN result displays erratic with large spikes and unusual curve shape.

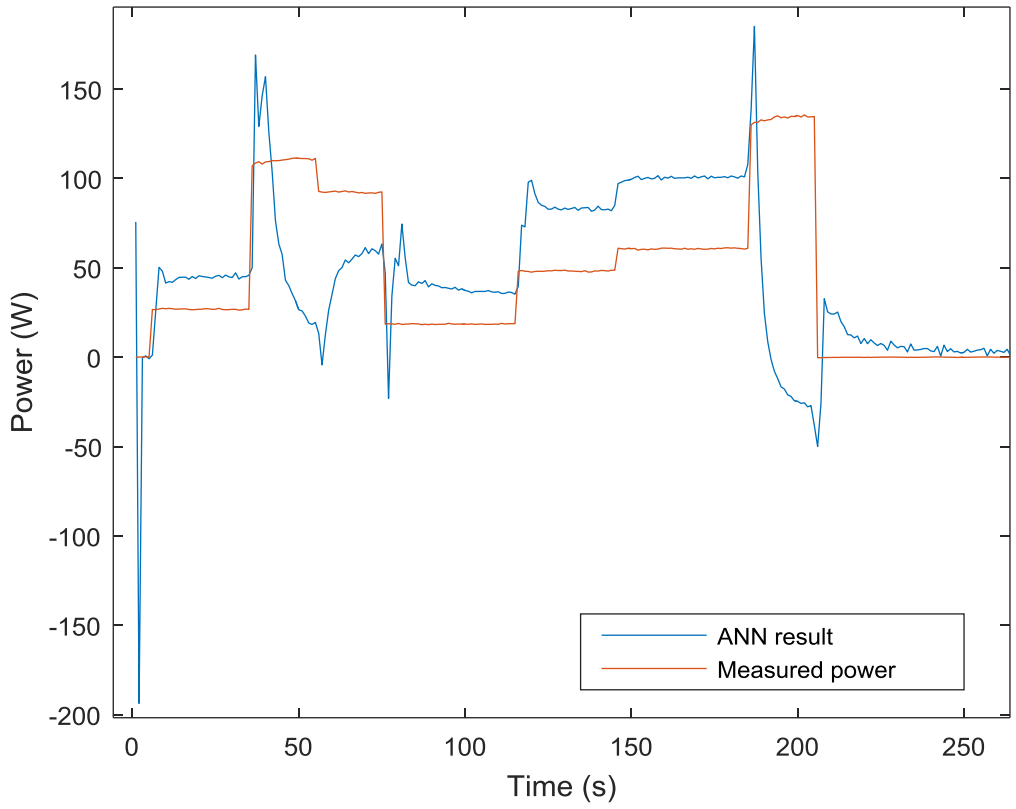


Figure 130. Comparison between power loss estimate for a severely degraded module (obtained using ANN train with healthy module data) and the measured power loss.

To recapitulate, through experiments with IGBTs dissipating power and ANN formed to model the dependency between that power and the external temperature rise it induces across the heat sink body, it has been discovered that the ANN can produce good power loss estimates, as long as the thermal system does not undergo a significant change. If such a change influences the change of

the heat flow path, then the ANN estimate of the power loss is no longer correct and the ANN needs to be changed or re-trained for the new conditions.

It must be noted that one of the possible reason for being unable to obtain close enough fit between the ANN estimate and the actual power loss may the fact that the experiments were conducted with severely degraded modules. Unfortunately, no modules with milder degradation (i.e. within the 20% R_{th} rise limit used by industry as degradation benchmark) were available for power loss and ANN experiments at that stage. But regardless of whether the ANN would have been able to provide more accurate estimates for mildly degraded modules, the experiment results still indicate that our initial idea for a practical health monitoring system may need to be revised and amended.

6.4 Re-evaluation of the Health Monitoring Method

The initial health monitoring concept explored here can be summarised by the process diagram in Figure 131. It uses existing electrical measurements from the converter controller to calculate from the datasheet what the healthy power losses (HPL) of the monitored power module should be for the thus defined converter operation point (at steady state). It uses a previously trained ANN as the tool for estimating what the actual operational power losses (OPL) of the converter are at that same point. It then compares HLP to OPL and uses the difference to determine the percentage of module degradation.

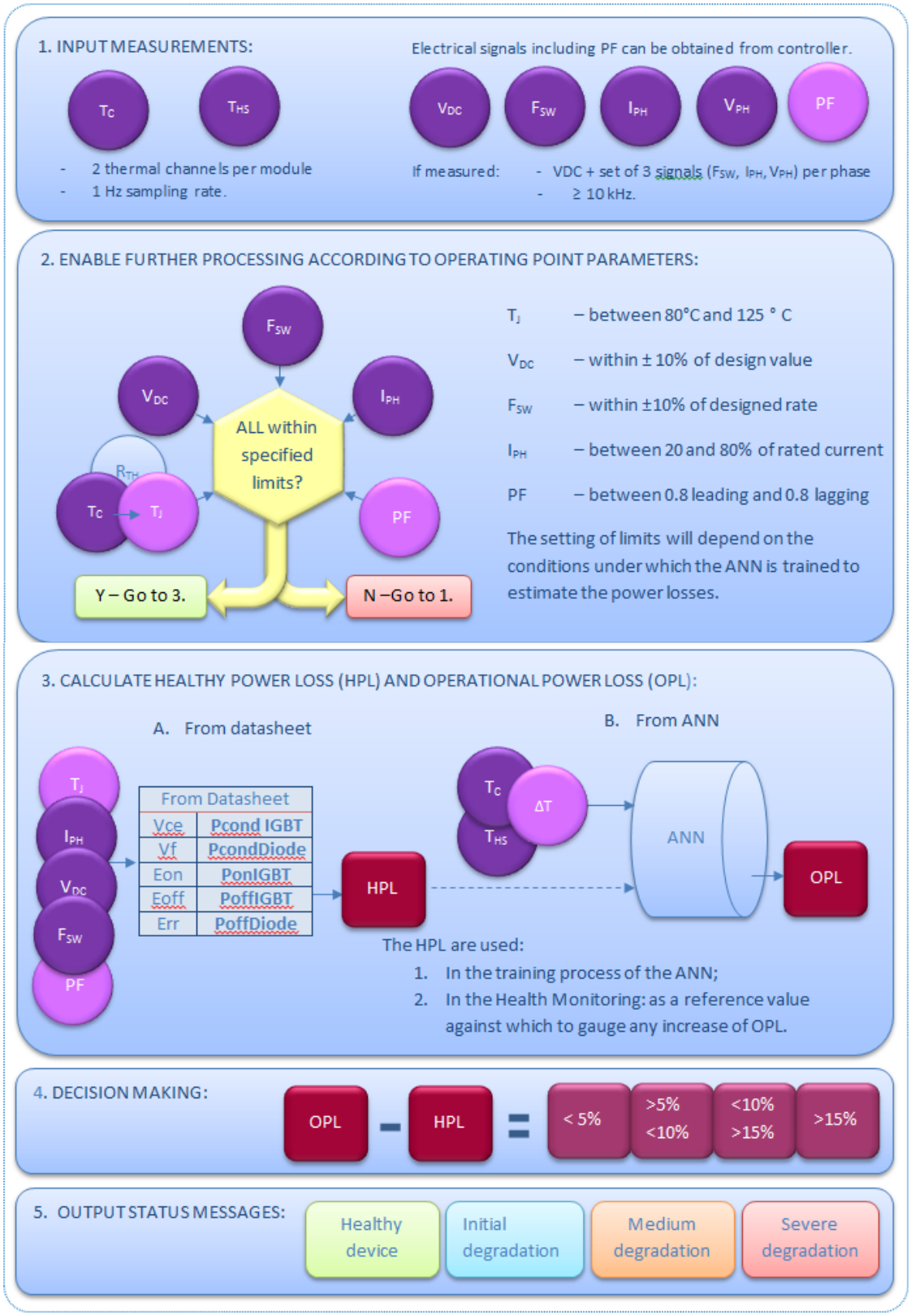


Figure 131. Proposed health monitoring process.

As the packaging module degradation is a gradual process, this monitoring method does not need to run at very fast rates. In fact, its algorithm includes (in stage 2 of the process) assessing the operating conditions and selecting appropriate period of time in which to be applied – to ensure it is performed during a window of time when the RMS currents and voltages of the grid and generator side have been stable for long enough to allow steady state operation on the thermal side as well. Using a dataset of signals acquired at this stable period of operation, the health monitoring algorithm then can proceed with the HPL and OPL estimation and comparison.

The experiments with IGBT modules, however, revealed that as the modules degrade overtime it will not be possible to rely on the estimate provided by the ANN trained in the initial healthy stage of the device's operational life. However, a new idea emerged based on the collected observations that for practical purposes it may be enough, if the health monitoring system can acknowledge degradation even without being able to determine accurately its level. For this reason, it will only be necessary to establish that the OPL estimated by the ANN differ significantly from what their expected level should be based on the HPL calculation.

A Hardware-In-the-Loop demonstration (performed when the project was still based at the ORE Catapult, Blyth) using case and heat sink datasets obtained from the IGBT experiments as simulated health monitoring system input confirmed that the above algorithm can indeed register such mismatch. However since the ANN used was not optimised for accuracy, there was also significant mismatch in the

HPL and OPL estimated in some case when the input consisted of healthy IGBT data. Such outcome is undesirable in commercial applications where the aim is to work the devices harder rather than exchange them unnecessarily when there is still sufficient life left in them. The onshore wind industry approach towards power electronics reliability – i.e. "change it when it breaks" – clearly demonstrates that.

The original idea of estimate comparison was also revisited from another angle. Two ANNs can be developed and run simultaneously. One, trained with data from the healthy new device at the start of its operation life, will model expected power levels in healthy condition operation. The other trained degraded device data will model the expected power losses in case of degradation. As the device degrades the difference between the two estimates, or their error, will be changing and it may be possible to calibrate the changes to degradation level of the device. Still, this concept has not been fully explored to ascertain whether using the error from 2 parallel running ANN will produce better power estimate for the degraded device and better assessment of the health condition. One of the biggest challenges here is to establish whether it is at all possible in a practical real-life scenario to create and train an adequate ANN corresponding to a yet unknown degraded condition. It is unclear how to produce or obtain realistic training data corresponding to a degraded module temperature and power loss, since they are converter-specific, mounting position-specific, mission-profile specific, etc. Also, as our experiments with degraded IGBT modules 2, 7 and d show, different degraded modules may exhibit may exhibit different thermal profiles while experiencing

similar power losses. If this reasons for this are better understood, then perhaps this idea having of simultaneous use of two ANNs – one based the healthy operation of the device and one based on a degraded condition – may be of practical use.

Existing IGBT experiment results can be further analysed to find further options, although – as pointed out their result validity may be restricted by the level of degradation and degradation mechanism.

Chapter

7 Conclusion and Suggestions for Further Work

7.1 Conclusions

To recapitulate, the goal of this project was to provide an industry-ready concept for power module condition monitoring that can be implemented with minimal design changes, expense and software complexity within the controllers of offshore wind turbine frequency converters, which can then offer its small but active contribution towards the lowering of the levelised cost of offshore wind energy.

Although compared to this grand goal, the project results appear now meagre, they still offer some contribution to science and industrial research and development in the fact that:

- The direction this project had set out to follow – i.e. condition monitoring based on external temperature measurements – has been further explored and the method initially suggested by the COMPERE project has been redefined and optimised in terms of the focus (power losses), the temperature measurements used (delta T case-to-heat-sink-reference point), the means for power loss estimation (ANN which allows temperature-to-power correlations in systems with multiple heat sources) and overall health monitoring algorithm including the effect of the electrical operating point of the converter.

- Extensive experimental work, aiming to emulate within reason and within the limited project resources the type of equipment and conditions in real-life converter systems (e.g. liquid-cooled cold plates, moderate junction temperatures, etc.), has yielded some new valuable practical observations (importance of device positioning which needs to be factored in the thermal modelling of the system, the initial condition of the packaging (e.g. the starting porosity within the die-attached solder layer), etc.

- The modelling done as part of this project also yielded some practically useful observations supporting experiments and providing an useful tool to exploring theoretically identified problems (e.g. unequal current sharing in parallel devices and the importance of their characteristic ZTC point, etc.)

The work on this project experienced peaks and troughs. There were extensive periods of time spent on trying to find alternative solutions the when planned one did not produce the expected results (e.g. the inability to achieve

accurate power loss modelling of degraded IGBTs based on ANN trained with data from their healthy operational condition), but in hind sight it could also be said that the explored directions which were found not to work, also contribute to science.

Overall, the project goal may have been overly ambitious given the starting point and resources, but this makes the humble new findings achieved here all the more valuable and it also opens a number of avenues for further research – something which is of value to science as well.

7.2 Suggestions for Further Work

As also pointed out in their relative chapters, the main aspects opened by this project for further work and research are as follows:

- Exploring the concept of condition monitoring using difference between expected and imperfectly estimated power losses as indicator of degradation, even though degradation level cannot be identified;
- Exploring further the concept of condition monitoring using two ANNs – one trained with healthy device data and the other one trained with degraded device data – which run in parallel and interpret the temperature signals in operation with a different level of error. The idea is to find out whether the change of this error level can be used to determine whether the device is closer to healthy or degraded condition.

- Continued work on the power cycling to achieve 20% R_{th} of modules which can be used in further experiments with ANN power loss estimation as well as for die-attach solder scanning;
- Further scanning and alongside FEA modelling to determine whether the proposed reason behind R_{th} increase (i.e. cracks rather than globular pores) can be confirmed.
- To continue exploration on multiple defects as opposed to single defects and understand their merging;
- Try to correlate the findings such as provided by the scan results and the parallel device modelling to the practical condition monitoring (e.g. sensor positioning, measuring and incorporating additional signals, etc.)

And finally, the power module packaging related problems investigated in this work are not the only aspects that can affect the reliability of the module and the system within which it operates. To put things in perspective, even if an industry deployable condition monitoring concept which works perfectly was fully developed here, it would tackle only one aspect of many that can go wrong. The "further" work of power electronics reliability engineers is never done.

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